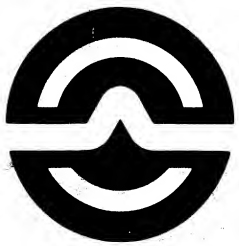
D-112 MSI 12-BIT DIGITAL COMPUTER

Installation and Maintenance Manual

Volume I



DIGITAL COMPUTER CONTROLS INC

SUPPLEMENT 1

to

D-112

INSTALLATION AND MAINTENANCE MANUAL

(VOLUME 1)

This supplement adds output connector data not included in the basic manual. The data for connector AØ6 in table 6-1 (bottom of left hand column) on page 6-5 is incomplete. The complete data for connector AØ6 is listed below.

CONNECTOR AØ6

D-112 PIN	SIGNAL	MNEMONIC
2	GRD	
4	LEVEL	DATA ADD ØØ*
6	GRD	
8	LEVEL	DATA ADD Ø1*
10	LEVEL	DATA ADD Ø2*
12	GRD	
14	LEVEL	DATA ADD Ø3*
16	LEVEL	DATA ADD Ø4*
18	GRD	
20	LEVEL	DATA ADD Ø5*
22	LEVEL	DATA ADD Ø6*
24	GRD	
26	LEVEL	DATA ADD Ø7*
28	GRD	
30	LEVEL	DATA ADD Ø8*
32	GRD	
5	GRD	
7	LEVEL	DATA ADD Ø9*
9	LEVEL	DATA ADD 1Ø*
11	GRD	
13	LEVEL	DATA ADD 11*
15	GRD	
17	LEVEL	BRKRQSTBUS*
19	GRD	
21	LEVEL	DATA IN
23	GRD	
25	LEVEL	BREAK*
27	GRD	
29	PULSE	BADDACCEP*
31	LEVEL	MEMINCR*
33	GRD	
35	PULSE	BINIT2

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SECTION I

GENERAL

1.0 INTRODUCTION

1.1 GENERAL

The purpose of this manual is to provide the field engineer with information necessary to install and maintain the D-112 minicomputer. The following sections include Theory, Operation, Installation and Maintenance Procedures. The reader should be familiar with digital logic circuitry, logic notation, TTL and MSI. For detailed information on these subjects a list of related documents is given in paragraph 1.3.

The D-112 is a general purpose, stored program, digital computer for application to information handling systems or as a control element in complex data processing systems.

1.2 FUNCTIONAL UNITS OF THE D-112

There are four basic functional elements of a stored program computer: an arithmetic unit, a control unit, a memory unit and an in/out unit. These basic functional units in the D-112 are described below.

1.2.1 Arithmetic Unit

The arithmetic unit is comprised of a set of 5 registers, steering circuits, (multiplexers), and an adder.

Arithmetic operations are performed by steering selected register contents into the adder inputs via 2 multiplexers. The adder output itself becomes one of the inputs to a data bus multiplexer. Other inputs to the data bus include: right or left shifted versions of the adder, a logical AND combination of the ACCUMULATOR (ACC) with the MEMORY BUFFER REGISTER (MBR), and an all-zeros signal for clearing.

The data bus accesses the 4 major registers: ACC, MBR, PROGRAM COUNTER (PC), and MEMORY ADDRESS REGISTER (MAR). The arithmetic unit also includes a Memory Data Register for transient storage of words from memory during a read-out. Data entry into a register is accomplished by applying a pulse from the Control Unit to the clock input of the register.

One cycle through the adder can produce the sum of the contents of any two registers, the right or left shifted version of the original contents of a register, complement the contents of certain registers, increment the contents of a register by adding a fixed "1" or clear any register.

The adder cycle time is short enough to permit several adder cycles to occur within one Memory Cycle.

Two kinds of arithmetic are performed. Ordinary operations are performed in 2's complement arithmetic. Negative numbers are formed by complementing a positive number and adding 1. This has the effect of raising negative zero to coincide with positive zero thereby avoiding the confusion that would result from having two values for zero. Logical arithmetic operations are also performed where the logical "AND", "OR" or "NOT" of a number is needed. These functions are used primarily in manipulating instructions.

1.2.2 Control Unit

The Control Unit determines what operations will be performed in each of the other units. It does this by sending appropriate levels to their gates and supplying selected timed pulses to cause clocking of registers and to initiate other events. It operates on the basis of stored instructions taken from the Memory during the previous cycle.

1.2.3 Memory Unit

The Memory Unit provides for the storage and retrieval of 12-bit words. Both instruction and data words are stored in Memory, instruction words usually being stored in successive locations in selected areas.

1.2.4 In/Out Unit

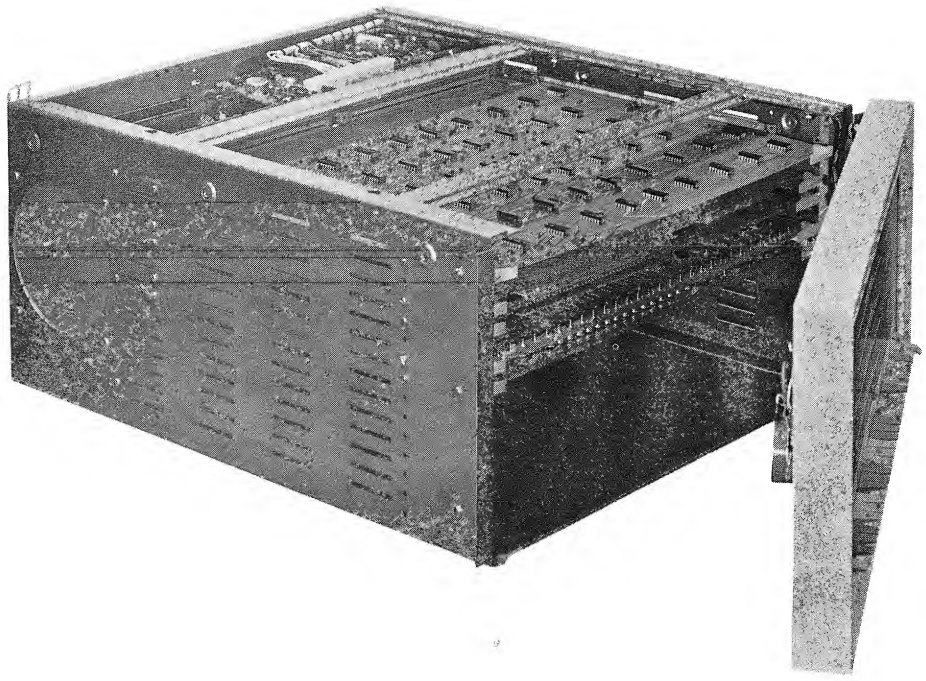
All information transfer into or out of the computer passes through the In/Out (I/O) Unit circuitry.

Since the computer operates entirely in binary electrical signals, all commands (such as START, STOP), indicators, switches, data from keyboard or punched tapes, etc., must be converted to properly timed uniform signals upon entry and, correspondingly, conversion to human usable form is needed in generating outputs. These functions are performed by the I/O Unit.

1.3 RELATED DOCUMENTS

The following documents serve as source material supplementing the information contained in this maintenance manual.

1. D-112 User's Handbook
2. Technical manual for the Teletype Unit, Automatic Send and Receive (ASR) Bulletin 273B, Volumes 1 and 2. This manual covers maintenance and operation of the Teletype Unit.
3. Bulletin 1184B contains and illustrates the parts breakdown to serve as a guide for disassembly, reassembly, and ordering of replacement parts for the Teletype Unit.



TOP

1	SPARE
2	I/O (+ OR –)
3	EX-ARITH
4	CU-1
5	CU-2
6	EX-MEM CONTROL
7	MEM-TIMING AND CONTROL
8	STACK 0
9	STACK 1
10	STACK 2
11	STACK 3
12	STACK 4
13	STACK 5
14	STACK 6
15	STACK 7

HINGE SIDE

FRONT VIEW

Assigned slots for Plug-in Printed Circuit (PC) Boards in Main Frame. Basic 4K configuration requires only 5 PC boards, 2, 4, 5, 7, & 8.

Figure 1-1. Component Board and Connector Board Interconnection

4. Instruction Manuals and Maintenance Programs as well as diagnostics provided for general maintenance by Digital Computer Controls, Inc.

5. Digital Computer Controls set of library documents, descriptive documents and perforated tape for the numerous programs available for use on the D-112 General Purpose Minicomputer.

2.0 DESCRIPTION

2.1 GENERAL

The D-112 is a fully parallel, 12-bit word computer with a memory cycle time of 1.2 microseconds.

The basic system includes 4096 words of Core Memory (usually referred to as "4K") with an an expansion capability of up to 32,768 words ("32K") within the main console (8 3/4" by 19" x 22"). Memory expansion is effected by plugging in a Memory Extension Control board and as many additional units of Core as is desired, in increments of 4096 words, up to the limit of eight boards providing a total of 32,768 words.

2.2 FEATURES OF THE D-112

Standard features include: indirect addressing, instruction skipping, program interrupt as a function of the input/output device requests, and 8 auto-index registers.

Memory protection against power failure is part of the basic system. Optional main-frame features include Data Break, Power Failure Detection and Restart, Memory Parity Control, Real Time Clock, Time Share and an Extended Arithmetic Unit. The Control Units for a standard Teletype Unit, a high-speed paper tape reader and a high-speed paper tape punch are also available as options within the main frame.

The I/O bus provided permits the connection of a wide variety of external I/O devices, including magnetic tape and disk units. The optional high-speed data channel allows peripheral devices to transfer large quantities of information at high rates.

The D-112 is built with MSI logic circuits. All circuit connections between the computer component circuit boards and the Core Memory boards are effected by a printed circuit connector board mounted in a plane 90 degrees perpendicular to the plug-in printed circuit computer and Core Memory boards. (See Figure 1-1 for Component board and Connector board interconnection.)

The 1.2 μs memory cycle of the D-112 enables it to perform an addition or subtraction in 2.4 μs using the computer's Accumulator. Multiplication can be performed by a softward subroutine in approximately 252 μs. Division performed by a similar subroutine requires approximately 355 μs. The Extended Arithmetic Unit Option performs Multiplication and Division in approximately 6.0 and 6.5 μs respectively.

2.3 SPECIFICATIONS

2.3.1 Electrical

Central Processor Unit -
Input: 115V ± 10V, 47-63Hz
@ 3 amperes for 4096 word memory
Power Dissipation: 300 watts

Teletypewriter -
Input: 115VAC ± 10%, 60Hz ± 0.45Hz,
@ 2 amperes
Power Dissapation: 150 watts

2.3.2 Environmental

Operational:	0°C to + 55°
Storage:	-10°C to +60°C
Humidity:	10 to 95% (no condensation)

2.3.3 Physical

Table-Top Model -	Dimensions: 9" high x 19" wide x 22" deep (supplied with outside cover)
Rack Mount Version-	Dimensions: 8.75" high x 19" wide x 22" deep (supplied with slides)
Weight	50 pounds
Teletypewriter ASR-33-	Dimensions: 33" high w/o copyholder x 23" wide x 18" deep
Weight-	70 pounds (including stand)

2.4 DETAILED FUNCTIONAL DESCRIPTION

Figure 1-2 is a functional block diagram.

The broad paths represent information flow. The single lines in the block diagram represent control function. Register control gating has been eliminated from the diagram for the sake of clarity. The block diagram also shows the Computer State Control Logic, which controls the setting of the main Computer States.

2.4.1 Major Registers

There are six major registers in the mainframe.

ACCUMULATOR (ACC) AND LINK (L)
PROGRAM COUNTER (PC)
MEMORY ADDRESS REGISTER (MAR)
MEMORY BUFFER REGISTER (MBR)
INSTRUCTION REGISTER (IR)
SWITCH REGISTER (SR)

ACCUMULATOR(ACC) - This 12-bit register is used for performing the arithmetic and logic

functions of the computer. Control Logic associated with the ACC enables an algebraic binary addition of the contents of a second register, the Memory Buffer Register (MBR), to the contents of the ACC, with the sum remaining in the ACC. Control logic also enables a Boolean Inclusive OR function to take place between the Switch Register (SR) and the ACC with the result remaining in the ACC. Finally, all program controlled data transferred between Core and an external device is buffered through the ACC.

LINK (L) - This is a flip flop used with the ACC to extend the range of arithmetic operations performed by the computer. When a carry out occurs in the ACC, the state of the L is complemented. This bit can be inspected by the program to check when overflow occurs, thereby simplifying and accelerating the single and multiple precision arithmetic routines. The L can be reset and complemented by the computer program and is rotated as part of the ACC.

PROGRAM COUNTER (PC) - The contents of this 12-bit register determine the location from which the next program instruction will be taken. The PC is manually loaded from the Switch Register (SR) by the computer operator. When executing a program, the PC is normally incremented by one with the fetching of each successive instruction word from the program in Core. However, when the instruction word calls for a jump-type operation, the PC is loaded with the address of the location to which it must branch.

MEMORY ADDRESS REGISTER (MAR) - This 12-bit register contains the address of the Core location being accessed at that time, either for fetching an instruction or for storing or retrieving data. The MAR can directly address 4096 Core locations. It is normally loaded from the PC. During indirect addressing, it is loaded from the MBR. The MAR can also be loaded by high-speed devices performing Cycle Steal transfers.

MEMORY BUFFER REGISTER (MBR) - This 12-bit register buffers all transfers of information between Core and the ACC and between Core and the MAR. Data can be transferred between Core and an external device performing Cycle Steal transfers by means of the MBR. Data from the Switch Register (SR) can be deposited in Core through the MBR.

SWITCH REGISTER (SR) - This 12-bit register is composed of manually operated switches located on the operator's console. When the LOAD ADD switch on the operator's console is depressed, the contents of the SR are loaded into the PC. When the DEP switch on the operator's panel is depressed, the contents of the SR are deposited in the Core through the MBR at the location specified by the PC. The SR can also be used to load information into the ACC by programmed means.

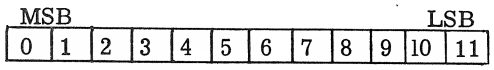
INSTRUCTION REGISTER (IR) - This 3-bit register contains the 3 most significant bits of the instruction currently under execution. After being loaded from the MBR, the information contained in the IR is decoded into one of the eight basic types of instructions.

2.4.2 Computer State Control Logic

The Computer State Control Logic assigns different computer states to successive computer cycles when executing program instructions and when performing Cycle Steal Data transfers with an external I/O device. The computer state assigned when executing a program instruction depends upon the instruction being performed and upon the current computer state. The states assigned for program instructions are Fetch, Defer, and Execute. The computer state assigned to Cycle Steal transfer operations is determined by request signals from the I/O device and by the computer's current state. The states assigned for Cycle Steal operations are Word Count, Current Address, and Data Break.

2.4.3 Core Memory

Core Memory consists of a memory timing and control PC board and from one to eight basic 4K memory stacks. The basic computer requires one stack. Up to seven additional stacks can be added using the Memory Extension Control option. Each Core Memory stack contains 4096 12-bit words and therefore requires twelve bits (0 through 11) to address all memory locations.



CORE MEMORY WORD

Core is addressed by lines from the MAR. All data to and from Core is transmitted over lines to the MBR. Bits are numbered from 0 to 11 according to the representation above. Bit 0 is the most significant bit (MSB) and bit 11 is the least significant bit (LSB).

3.0 OPERATION

3.1 GENERAL

This section will identify all controls and indicators used for operating the D-112, including the ASR-33 Teletypewriter usually supplied as the basic I/O device.

3.2 D-112 CONTROL PANEL

Figure 1-3 shows the front panel of the computer. The functions of its controls and indicators are described in Table 1-1. The following switches and lamps, although physically present in the panel, are functional only when the corresponding option is included in the Unit:

CONTROL INDICATOR	OPTION
DATA FIELD (SWITCHES & LAMPS)	MEMORY EXTENSION
INST FIELD (SWITCHES & LAMPS)	MEMORY EXTENSION
STEP COUNTER (LAMPS)	EXTENDED ARITHMETIC

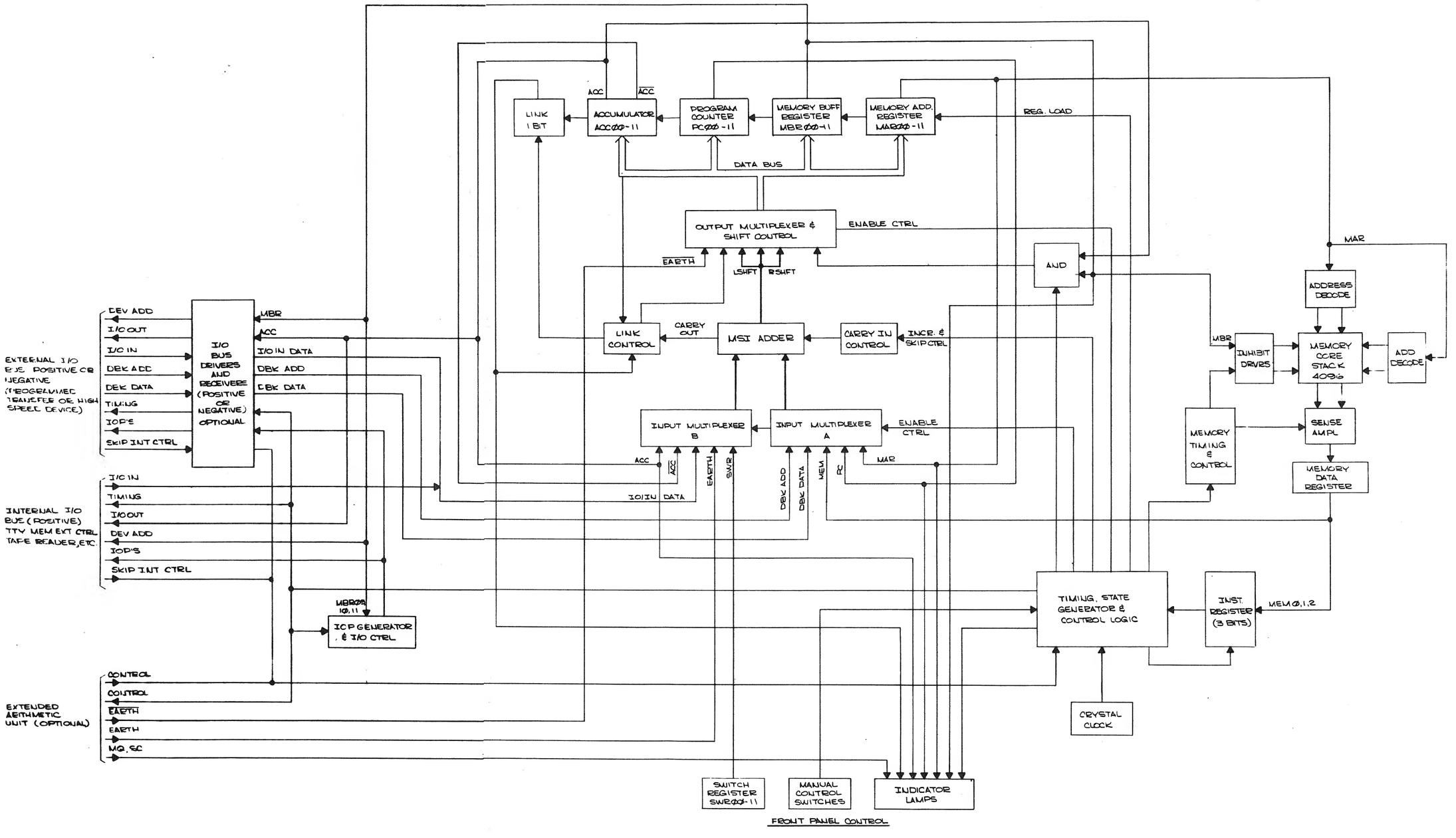


Figure 1-2. D-112 Functional Block Diagram

CONTROL INDICATOR	OPTION
MULTIPLIER/QUOTIENT (LAMPS)	EXTENDED ARITHMETIC
WORD COUNT (LAMP)	DATA BREAK
CURRENT ADDRESS (LAMP)	DATA BREAK
DATA BREAK (LAMP)	DATA BREAK
PARITY (LAMP)	MEMORY PARITY

Two of the options mentioned above contain registers which are referred to in Table 1-1. They are the following:

Memory Extension Control option:
Data Field Register (DFR)
Instruction Field Register (IFR)

Extended Arithmetic Unit:
Step Counter Register (SCR)
Multiplier/Quotient Register (MQR)

These registers are present only if the corresponding option is included in the equipment configuration.

3.3 TELETYPE CONTROLS

The ASR-33 Teletype controls are shown in Figure 1-4. The functions of its controls are described in Table 1-2.

3.4 LOADING INFORMATION INTO CORE

Information can be loaded into the computer core memory either manually (by making use of the facilities in the Control Panel) or automatically (by making use of a program previously loaded into core). This second approach is much more efficient than the first and is the procedure normally utilized, but when no program exists in memory there is no option to manually loading the the first one.

Programs that can load other Programs into Core are called Loaders. The Manual procedure is usually limited to loading the RIM Loader, which is a program whose only function is to load into Core other Programs that exist in RIM-formatted perforated tape.

Two versions of the RIM Loader are used. One is used with the ASR-33 Perforated Tape Reader (Low Speed Reader) and the other is used with the Photo-electric (High Speed) Tape Reader.

3.4.1 Rim Loading Procedure

To load the RIM in Core perform the following steps: (All switches referenced are on the D-112 Control Panel.)

a. Set OFF-POWER-PANEL LOCK switch to POWER.

b. Set the MEM PROT switch to the down position.

c. Set the value 7756_8 into the SWITCH REGISTER.

d. Press LOAD ADDR switch and monitor the PROGRAM COUNTER indicator lamps which confirm the loading of the 7756_8 address into the PC.

e. Set into the SWITCH REGISTER the value of the first instruction of the Program (6032_8 if using the Low Reader or 6014_8 if using the High Speed Reader).

f. Press the DEP keyswitch and monitor the MEMORY BUFFER indicator lamps which confirm the loading of the instruction into the Core location specified by the PC.

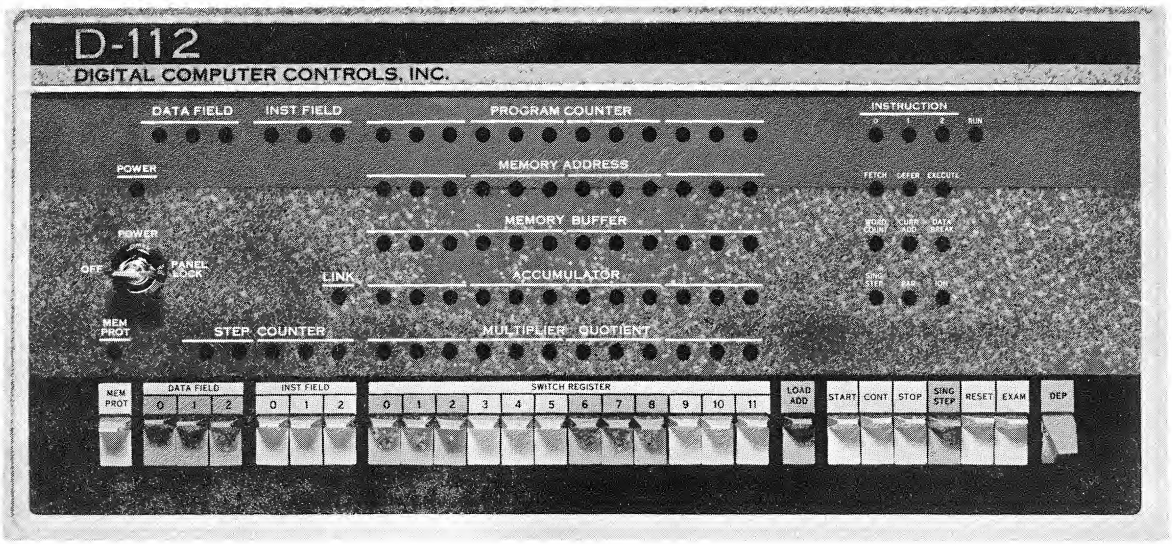


Figure 1-3. D-112 Control Panel

Table 1-1. Functions of Controls and Indicators for D-112 Control Panel

CONTROL OR INDICATOR	FUNCTIONAL DESCRIPTION
OFF-POWER-PANEL LOCK (KEY SWITCH)	In the OFF position this switch removes all power from the computer. In the POWER position the computer is supplied with power for all functions. When in the PANEL LOCK position the power is supplied to the computer for operation, but all manual control switches are disabled except the SWITCH REGISTER and the DATA FIELD and INST FIELD switches.
MEM PROT (SWITCH)	When this switch is in the up position it protects the last page of memory from being modified. This includes all addresses between 7600_8 and 7777_8. When in the down position this switch permits writing in these addresses. When more than one module of Core memory is used in the computer this switch always protects the last page of the Core module with the highest field number.
DATA FIELD (SWITCHES)	This group of three switches is used to load information into the DFR of the Memory Extension Control option. The contents of the DF switches are transferred into the DFR when the LOAD ADDR key is depressed.
INST FIELD (SWITCHES)	This group of three switches is used to load information into the IFR of the Memory Extension Control option in a manner identical to the preceding case.
SWITCH REGISTER (SWITCHES)	This group of twelve switches enables the loading of 12-bit words into the PC and memory (through the MBR). The SR can also be accessed by a running program, serving as a means of communicating with it.
LOAD ADDR (SWITCH)	This switch is used to transfer the contents of the SWITCH REGISTER into the PC, and of the DATA FIELD and INST FIELD switches into the DFR and IFR, respectively, when present.
START (SWITCH)	This switch initiates program operation by clearing the program interrupt control circuits, the ACC and L, by causing the Computer State Control Logic to produce the Fetch state and by enabling the computer timing circuits to operate.
CONT (SWITCH)	This switch is used to set the RUN flip flop to continue the program according to the computer state and instruction decoded at the address specified by the PC. The ACC and L are not cleared by this switch.
STOP (SWITCH)	This switch resets the RUN flip flop at the end of the instruction being executed when it is pressed.
SING STEP (SWITCH)	When this switch is in the down position the program is executed one memory cycle at a time so that the operator can observe the contents of every register as displayed by the control panel indicator lamps.
RESET (SWITCH)	When this switch is pressed it produces a signal similar to the power clear signal produced in the computer. This clears the shift register timing generator, the

Table 1-1. Functions of Controls and Indicators for D-112 Control Panel (cont)

CONTROL OR INDICATOR	FUNCTIONAL DESCRIPTION
RESET (Cont)	Computer State flip flops and the RUN flip flop. It can also be used by peripheral devices connected to the I/O bus as a clear signal.
EXAM (SWITCH)	This switch transfers the contents of the memory location specified by the PC (and the IFR, if present) into the MBR. The address contained in the PC is then incremented by one to allow the examination of the contents of sequential memory locations, by repeated operation of the EXAM switch. This switch also clears the Computer State Control flip flops.
DEP (SWITCH)	This switch transfers the contents of the SWITCH REGISTER through the MBR into Core memory at the address specified by the PC (and the IFR, if present). The contents of the PC are incremented by one each time the DEP switch is operated. This produces storage of information in sequential memory locations.
DATA FIELD (LAMPS)	These indicator lamps show the contents of the DFR of the Memory Extension Control option, which is used to access memory for data during execution of indirectly-addressed AND, TAD, ISZ and DCA instructions.
INST FIELD (LAMPS)	These indicator lamps show the contents of the IFR, which acts as an extension of the PC when the Memory Extension Control is included in the configuration.
PROGRAM COUNTER (LAMPS)	These indicator lamps show the contents of the PC. During Program execution the PC (together with the IFR, if present) specifies the memory address of the next instruction to be executed.
MEMORY ADDRESS (LAMPS)	These indicator lamps show the contents of the MAR which contains the address of the memory location that is being accessed by the D-112.
MEMORY BUFFER (LAMPS)	These indicator lamps show the contents of the MBR which holds the contents of the memory location last addressed by the MAR.
ACCUMULATOR (LAMPS)	These indicator lamps show the contents of the ACC.
LINK (LAMP)	This lamp shows the state of the link bit.
MEM PROT (LAMP)	This lamp lights to indicate a memory protect violation when an attempt is made to write into the protected last page of Core if the MEM PROT switch is up. The computer will then halt its operation.
STEP COUNTER (LAMPS)	These indicator lamps show the contents of the SCR used in the Extended Arithmetic Unit. The SCR stores the complement of the contents of bits 7-11 of the memory location following the location of the Extended Arithmetic Instruction by which it was loaded. It also contains the exponent after an NMI instruction. It is set to zero after a DVI or MUY instruction.
MULTIPLIER QUOTIENT (LAMPS)	These indicator lamps show the contents of the MQR used in the Extended Arithmetic Unit. The MQR stores the multiplier at the beginning of a multiplication instruction and stores the least significant half of the product at the

Table 1-1. Functions of Controls and Indicators for D-112 Control Panel (Cont)

CONTROL OR INDICATOR	FUNCTIONAL DESCRIPTION
MULTIPLIER QUOTIENT (LAMPS) (Cont)	end of multiplication. It also stores the least significant half of the dividend at the start of a division and at the end it holds the quotient.
INSTRUCTION 0, 1, 2 (LAMPS)	These indicator lamps show the contents of the IR.
RUN (LAMP)	This lamp lights when the RUN flip flop is set.
FETCH (LAMP)	This lamp lights when the FETCH flip flop is set, signifying that the computer is in the Fetch state.
DEFER (LAMP)	This lamp lights when the DEFER flip flop is set signifying that the computer is in the Defer state.
EXECUTE (LAMP)	This lamp lights when the EXECUTE flip flop is set signifying that the computer is in the Execute state.
WORD COUNT (LAMP)	This lamp lights to indicate that the Word Count state is in effect during a Cycle Steal operation.
CURR ADD (LAMP)	This lamp lights to indicate that the Current Address flip flop is set and that the Current Address state is in effect during a Cycle Steal operation.
DATA BREAK (LAMP)	This lamp lights to indicate that tne computer is in the Data Break state during a Cycle Steal operation.
SINGLE STEP (LAMP)	This lamp lights to indicate that a single step operation is being performed using the SING STEP switch.
PAR (LAMP)	This lamp lights to indicate that a parity error has occurred. The lamp is only functional when the Memory Parity Control option is installed.
ION (LAMP)	This lamp lights to indicate that the interrupt feature of the computer is enabled.

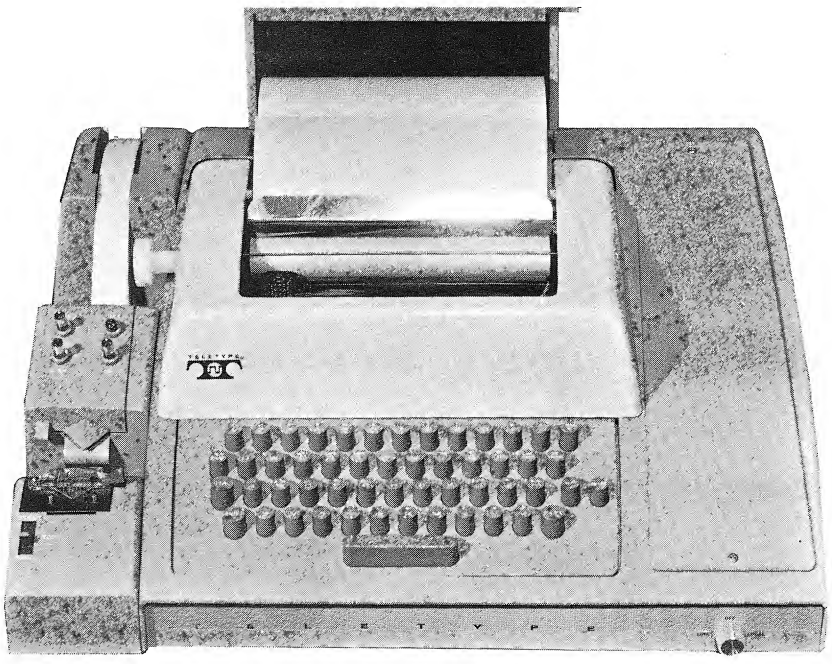


Figure 1-4. ASR-33 Teletype

Table 1-2. Functions of Controls for ASR-33 Teletype

CONTROL	FUNCTIONAL DESCRIPTION
LINE/OFF/LOCAL (SWITCH)	This switch controls the application of AC power to the Teletype and the Data Control Adapter for computer operation. When in the LINE position the Teletype power is on and the Teletype is connected to the Computer as an I/O device and operates under program control. In the LINE position data generated from the keyboard (or from the Tape Reader if the START/STOP/FREE switch is in the START position) will be supplied to the computer, and data from the computer will be supplied to the printer (and to the Tape Punch if the ON pushbutton is depressed) through the I/O bus. When the switch is in the OFF position the AC power is removed from the Teletype. When in the LOCAL position the AC power remains on but the Teletype is in an Off-Line mode being disconnected from the I/O bus.
KEYBOARD	When the LINE/OFF/LOCAL switch is in LOCAL the keyboard prints on paper as a typewriter and will cause tape to be punched if the punch control ON pushbutton switch is actuated. When the LINE/OFF/LOCAL switch is in LINE the keyboard provides computer input data to the I/O bus under program control.
OFF and ON (PUSHBUTTONS)	These pushbutton controls are used for the Tape Punch. When the ON pushbutton is actuated while the LINE/OFF/LOCAL switch is in LINE, computer output data being typed by the printer also punches a tape. When the ON pushbutton is actuated while the LINE/OFF/LOCAL switch is in LOCAL the tape can be punched from the keyboard. The OFF pushbutton disables the punch from keyboard or I/O operation.
REL. (PUSHBUTTON)	This pushbutton releases the tape in the punch to enable the loading or removal of the tape.
B. Sp. (PUSHBUTTON)	Depressing this pushbutton back spaces the tape in the punch by one space enabling correction or deletion of the last character punched.
START/STOP/FREE	This switch controls the use of the Tape Reader in the Teletype. When in the FREE position the tape is disengaged and can be loaded or unloaded. In the STOP position the reader is deenergized while the tape remains engaged. In the START position the reader is energized. In this position it can be operated either under program control (if the LINE/OFF/LOCAL switch is in LINE) or in an off-line mode (if the switch is in LOCAL).

g. Continue to load instructions with the values listed in the Program listing using the procedures outlined in steps e and f until the last instruction at loc. 7775 has been entered (loc. 7776 is a working location for RIM and need not be loaded).

3.4.2 ASR-33 Teletype Operating Procedures

The ASR-33 Teletype unit can be used to load tapes in RIM format into Core after the ASR-33 RIM loader program has been loaded.

3.4.3 Procedure for Loading Punched Tape Programs

To load a tape program in RIM format from the Teletype perform the following steps:

a. Set the OFF-POWER-PANEL LOCK switch on the D-112 Control Panel to the POWER position.

b. Set the Teletype LINE/OFF/LOCAL switch to the LINE position.

c. Set the START/STOP/FREE switch on the Teletype to the FREE position.

d. Release the tape cover guard with the latch to the right of the guard and align the tape feed holes with the sprocket teeth.

e. Close the tape cover guard and move the tape toward the front of the Teletype until the tape leader is over the reader unit.

f. Set the START/STOP/FREE switch on the Teletype to STOP.

NOTE

When the operator faces the keyboard in his normal operating position he should observe three tape hole positions to the left of the sprocket and five tape hole positions to the right of the sprocket.

g. Load the starting address of the RIM loader (7756_8) into the PC, using the D-112 SWITCH REGISTER and LOAD ADDR key switch.

h. Set the MEM PROT switch on the D-112 Control Panel to the down position.

i. Press the START pushbutton switch on the D-112 Control Panel.

j. Set the START/STOP/FREE switch on the Teletype unit to START.

k. When the tape has been read, depress the STOP switch on the D-112 Control Panel.

3.4.4 Binary Loader

Binary Loader (BIN) is a loader program that exists in RIM-formatted tape. It can, therefore, be read into Core by RIM. Once in Core it is used to load programs that exist in BIN format, which is more flexible and efficient than RIM format. The procedure to load into Core a BIN-formatted tape (referred to as a binary tape) is similar to the one described above, the main difference being that the starting address of BIN (7777_8) is used instead of the starting address of RIM (7756_8). For a detailed description of the operating procedure see the Binary Loader manual.

3.5 TELETYPE TAPE PUNCHING PROCEDURE

The Teletype can be used Off-Line to punch original tapes and duplicates of existing tapes.

RIM LOADER

ADDRESS	LOW SPEED READER INST'N.	LOW SPEED READER MNEMOMIC	HIGH SPEED READER INST'N.	HIGH SPEED READER MNEMONIC
7756	6032	KCC	6014	RFC
7757	6031	KSF	6011	RSF
7760	5357	JMP.-1	5357	JMP.-1
7761	6036	KRB	6016	RRB RFC
7762	7106	CLL RTL	7106	CLL RTL
7763	7006	RTL	7006	RTL
7764	7510	SPA	7510	SPA
7765	5357	JMP.-6	5374	JMP.+7
7766	7006	RTL	7006	RTL
7767	6031	KSF	6011	RSF
7770	5367	JMP.-1	5367	JMP.-1
7771	6034	KRS	6016	RRB RFC
7772	7420	SNL	7420	SNL
7773	3776	DCA 1 .+3	3776	DCA 1 .+3
7774	3376	DCA.+2	3376	DCA.+2
7775	5356	JMP.-17	5357	JMP.-16
7776	0000	Ø	0000	Ø

3.5.1 Original Tape Preparation Procedure

To punch an original program tape perform the following steps:

a. Set the OFF-POWER-PANEL LOCK switch on the D-112 Control Panel to POWER.

b. Set the Teletype LINE/OFF/LOCAL switch to LOCAL.

c. Raise the tape cover on the teletype punch and direct the tape through the guides at the back of the punch.

d. Feed the tape through the punch using the friction wheel.

e. Close the punch cover.

f. Energize the punch by depressing the ON pushbutton on the Teletype.

g. Produce about 2 feet of leader on the tape by punching either 200_8 or 377_8.

NOTE

200_8 is produced by holding down the CTRL and SHFT keys with the left hand. With the right hand hold down the REPT key and press the @ key for as long as it takes to produce the leader. Release the @ key before the other keys. 377_8 is produced by holding down the REPT and RUB OUT keys until the required amount of leader has been produced. To produce blank tape (and also as an alternative to fee the tape through the punch) proceed in the following way:

a. Depress the punch OFF pushbutton.

b. Depress the Teletype BREAK key.

c. Depress the punch ON pushbutton.

d. When enough tape has been produced, depress the punch OFF pushbutton.

e. Release the BREAK key.

3.5.2 Duplicate Tape Preparation Procedure

To prepare a duplicate punched tape load a blank tape in the punch and prepare a leader as when preparing an original tape. Then load the tape being duplicated into the reader as described in the procedure for loading tapes from the Teletype. Initiate operation by setting the Teletype LINE/OFF/LOCAL switch to LOCAL and the Reader START/STOP/FREE switch to START. The punch stops when the tape is read.

SECTION II

THEORY OF OPERATION

1.0 GENERAL

This section covers the detailed theory of operation of the D-112 Minicomputer. Refer to VOLUME II of the Maintenance Manual for detailed logic diagrams.

2.0 ORGANIZATION OF THE COMPUTER

The functional block diagram shown in Fig. 1-2 identifies the major elements of the four basic units: Arithmetic Unit, Control Unit, Memory and I/O Unit. Also shown are the Front Panel Controls and Indicators that provide the direct interface with a human operator. The I/O unit provides both 'internal' and 'external' busses. The console Teletype (TTY) accesses the computer through the 'internal' I/O bus; peripheral devices access through the 'external' bus. The Timing and State Control logic are elements of the Control Unit (CU-1), the Main Registers are associated with the Arithmetic Unit (CU-2).

2.1 FRONT CONTROL PANEL

The front panel switches and indicator lamps allow the operator to insert information into the computer, control the operation of the computer and ascertain the internal status. The Front Control Panel consists of three main sections: (a) the Switch Register (SR); (b) the Manual Control Switches; and, (c) the Indicator Lamps. The information contained in the SR can be stored either in the Memory Buffer Register (MBR) or the Memory Address Register (MAR) by means of the manual control switches (LOAD ADD, DEP). This procedure enables the operator to load a program starting address or store information in a particular memory location. The Indicator Lamps display the binary digits stored in all main registers simultaneously. (A detailed description of the function of each switch and indicator lamp was given in Section I.)

2.2 TIMING, STATE GENERATOR AND CONTROL LOGIC

This section of the computer generates all the timing signals, state control and state signals necessary for computer operation. It also generates the register load signals and controls the enable selection of signals for the input and output multiplexers of the arithmetic unit.

The control logic receives information from the instruction registers, memory buffer registers, accumulator, I/O bus, and manual control switches. A Crystal Clock supplies precise timing pulses for the control logic and computer timing.

2.3 ARITHMETIC UNIT (CU-2)

The central element of the Arithmetic unit is a MSI 12-bit adder. The control logic determines which of the input signals to the multiplexers designated A and B will be fed to the 12-bit adder. The different signals that may be applied to each multiplexer are shown in Figure 1-2.

The output of the adder is one input to the data bus multiplexer, which has the double function of transferring information from the adder to the register data bus, or providing the means for a right or left shift of the information to the register. The data bus feeds the inputs of all registers in the computer.

The Carry into the Adder is controlled by the carry control. This control provides the means to increment any information being transferred through the adder and also enables a "skip" under program control.

The Carry out from the Adder is handled by the link control providing control for the 2's complement arithmetic. The link control also provides information in the right/left shift operation when the link is shifted with the accumulator bits.

Data from the arithmetic section output multiplexer is fed directly into the four main registers.

2.3.1 Example of Adder Operation

The addition of two binary numbers, or the transfer of information through the adder, is accomplished in a complement mode. This means that, when two binary numbers are added, their complements are applied to the input of the adder and the CARRY IN signal is enabled. The results of this addition is then inverted by the output de-multiplexer before it is enabled by the data bus into the input of the main registers. A typical example for the addition of two numbers is shown on page 2-2. For a transfer of information from one register to the other, the multiplexer that is not transferring the register information supplies logical ones to the 12-bit input of the adder, the Carry is enabled and the transfer takes place. The transfer from one register into the other is shown in the example on page 2-2. At the time of transfer of information from one register into the other an increment order is given, the CARRY IN is set to zero, and the increment takes place. The carry out from bit ØØ of the adder is inverted in order to provide the actual carry out logic level.

2.4 MAIN REGISTERS

ACCUMULATOR (ACC). This 12-bit register is used chiefly with the arithmetic and logic operations. The ACC stores the results of these operations after they have been performed. It is also used as an intermediary register for the I/O programmed data transfers.

PROGRAM COUNTER (PC). This 12-bit register contains the address of the memory location of the instruction that the computer is going to execute.

MEMORY ADDRESS REGISTER (MAR). This 12-bit register contains the address of core memory that is currently being accessed in the memory operation (Reading or Writing). The 12-bits of MAR permit the direct addressing of 4096 words of memory.

Example

ACC	101	000	111	010	(MULTPX B)	NORMAL ADDER
MEM	010	110	101	101	(MULTPX A)	
CARRY OUTPUT = 0	111	111	100	111	(ADDER OUTPUT)	
ACC	010	111	000	101		COMPLEMENT MODE ADDER
MEM +	101	001	010	010	Carry in = 1	
CARRY OUTPUT = 1	000	000	011	000		
Complementing 0	111	111	100	111		
MEM	011	011	100	001		REGISTER TRANSFER
$\overline{\text{MEM}}$	100	100	011	110		
MLTPX B +	111	111	111	111	Carry in = 1	
CARRY OUTPUT = 1	100	100	011	110		
Complementing 0	011	011	100	001		

MEMORY BUFFER REGISTER (MBR). This 12-bit register contains all the data that is being transferred into or out of core memory. During the read portion of the memory cycle, the MBR stores the information read from the core memory. In the write portion of the cycle the MBR stores either new information supplied by the computer or the same information received from the MBR during the read portion of the cycle. The MBR also supplies information to the control logic section and the address for selection of devices on the I/O bus.

LINK (L). The Link is a 1-bit register that extends the logic arithmetic capabilities of the accumulator. It is used as a carry register for 2's complement arithmetic, also providing one extra bit in the shift operations of the ACCUMULATOR.

2.5 CORE MEMORY AND ASSOCIATED REGISTER AND CONTROL SIGNALS

As indicated in the block diagram (Figure 1-2) the core memory is composed of the Core Stack, Address Decoder, Sense Amplifiers and Inhibit Drivers. The Address Decode section receives information from the MAR, which is decoded to provide X and Y driver signals, forming a matrix to select core addresses. The Inhibit Drivers receive information from the memory buffer register and provide the means to place new information into core memory during the write portion of the memory cycle. The Sense Amplifiers receive information during the read section of the memory cycle, and supply this information to the memory data register. The memory data register supplies the new information directly into multiplexer A of the computer.

The memory timing and control section supplies all timing signals necessary for memory operation. This section receives the enable read and write commands directly from the timing and state generator control logic of the computer.

The first three bits in the memory data register are stored in the instruction register for use in determining which of the computer instructions are to be executed.

2.6 I/O UNIT

The I/O section is divided into three main parts:

2.6.1 External I/O Bus

The external I/O bus provides the necessary driver and receiver circuits to interface with all peripheral devices. This circuitry is specifically designed for matching the impedance, speed and drive requirements of the cables to the I/O. The receiver section is designed to provide noise immunity in environments to which the I/O is subjected. The main signals supplied by the External I/O bus are:

Device Address — The Device Address is comprised of 12 different signals, six are true, and

the other six are their complements. Accordingly, it is possible to address up to 64 peripheral devices connected to the I/O bus. These signals provide the means for transferring information to and from the I/O bus through the accumulator of the computer.

DBK, ADD and DBK Data signals provide the means for controlling the data break address lines and data break data lines into the computer. The control logic provides the internal timing and state of the computer to the data break and I/O devices. The IOP generator provides three different timing signals to the I/O devices for micro control. Finally, the skip and interrupt control supplies the computer with the interrupt request and skip request from the peripheral devices. The external bus is positive logic, where the signals are between ground and +3 volts. A negative I/O bus option is offered where the signals are between ground and -3 volts.

2.6.2 Internal I/O Bus

The internal I/O bus is used with all device controllers and options housed in the main frame of the computer. It is always a positive bus and supplies the same signals as those fed to the external I/O.

Typical options used with the internal I/O bus are the teletype interface, the memory extension control, the high speed paper tape reader, high speed paper tape punch, etc.

2.6.3 IOP Generator and Control

This section generates the IOP timing pulses. It also supplies control for the timing signals going to the I/O bus or coming from the I/O bus into the control logic. The IOP generator timing is adjustable.

2.7 SPECIAL OPTIONS

It is also indicated in the block diagram (Figure 1-2) that the computer supplies control signals and timing functions for special options such as the Extended Arithmetic Unit.

Several control signals are fed to the extended arithmetic section from the timing and state control logic; also, control signals which originate in the arithmetic unit are fed to the timing and state control logic. A direct input to the adder section multiplexer B and the output multiplexer is provided.

The front panel has indicator lamps for the MULTIPLIER QUOTIENT (MQ) register and STEP COUNTER (SC) register. The lamps indicate the status of the MQ and SC registers when the Extended Arithmetic option is incorporated. Detailed descriptions of the Extended Arithmetic Unit, Time Sharing Option and other possible options that may be incorporated into the D-112 computer are supplied together with Logic Diagrams when the option is ordered by the customer.

3.0 DETAILED FUNCTIONAL DESCRIPTION

3.1 COMPUTER TIMING

The computer timing generator supplies all the timing signals necessary for the logic operation of the processor. The generator consists of a crystal clock, a frequency divider and a shift ring counter. The ring counter shifts one bit at a time when in operation. The seven bits of the shift counter are divided into two sections. The first section of three bits provides the manual timing operation, and the second section of four bits provides the regular computer timing signals. The first section (for the manual timing) supplies three level signals, called LM1, LM2, and LM3. They in turn generate three timing pulses called PM1, PM2, and PM3. The second section of four timing bits provides levels called LT1, LT2, LT3, and LT4. These signals then generate the timing pulses PT1, PT2, PT3, and PT4. The width of the timing pulses is 75 nanoseconds.

When any of the control switches on the front panel is operated the following sequence occurs: The start flip-flop STFF is set thereby starting the ring counter by setting the LM1 Timing flip-flop for one clock period. In order to avoid any switch bounce effects or possible interaction between manual switches and the computer controlled functions every switch in the front panel controls a flip-flop circuit. This flip-flop insures positive operation at the correct time. The contents of the LM1 flip-flop is then shifted one step into the next flip-flop of the shift register. (The first three timing signals as noted previously correspond to LM1, LM2, LM3 Manual Functions.) The bit is then shifted into the regular LT timing counter of the Processor. If single cycle operation is required (as in the case of Load Address, or Deposit) the bit is shifted up to the LT4 flip-flop in the ring counter. The computer then stops with the timing signal LT4 high, and PT4 not issued. If the computer is set to RUN under the control of the Start or Continue switch, PT4 is then issued and LT4 is shifted back to the first flip-flop of the regular timing, LT1. The shift counter continues operating until the RUN flip-flop is reset.

The main timing diagram of the D-112 is shown in Figure 2-1.

3.2 COMPUTER STATES

The D-112 has three main states and three secondary states. The three main states are FETCH, DEFER, and EXECUTE. The FETCH state always occurs prior to the execution of any instruction. The DEFER state is used only for instructions requiring indirect addressing. The EXECUTE state is used for instructions which require two memory cycles for their execution.

The three secondary states are Data Word Count (DWC), Data Current Address (DCA), and Direct Data Transfer (DDT). These three states are explained in detail in Section 4.5 wherein the Data Break Option is described.

All states in the computer are cleared at LM1 time whenever any control key is activated with the exception of Continue. This clear signal is called MANPRES.

When the start key is pressed the START signal is generated at PM3 time. This signal sets the Fetch state of the computer. After that the processor always decides which state is to be executed next. The state transition of the computer takes place at the leading edge of the PT4 timing pulse. The different states of the computer are explained in detail at the same time that the Instructions are described.

3.3 MANUAL FUNCTIONS

The front panel of the D-112 minicomputer provides several switches which initiate manual

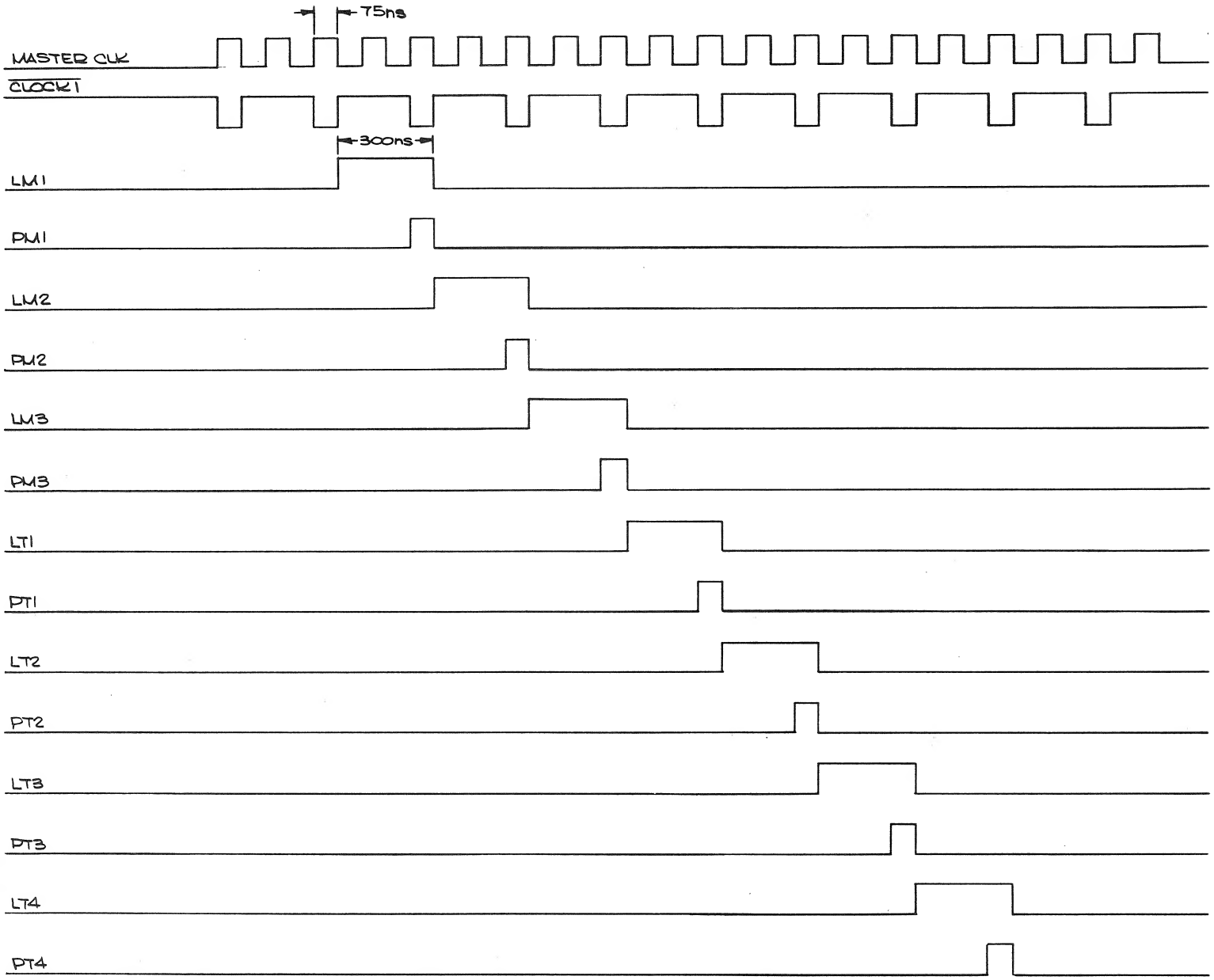


Figure 2-1. D-112 Timing Diagram

operations. These switches are: START, STOP, LOAD ADDRESS, CONTINUE, EXAMINE, DEPOSIT, SINGLE STEP, CLEAR and MEMORY PROTECT. Several other switches have been detailed earlier in this Chapter, such as the Switch Register, as well as the Data and Instruction Field Switches.

The control switches can be operated one at a time or in combination. This permits manual intervention into the program for writing and reading in a selected memory address location. Most of the control switches operate only when the computer is not running. An exception is the stop switch which is active only at run time.

The following are detailed descriptions of the logical operations that occur when a control switch is operated.

LOAD ADDRESS KEY (K-LA). When this switch is pressed the signal K-LA is generated in the computer. This signal sets the STFF flip-flop that starts the timing generator of the computer. During the LM1 timing, the MANPRES signal is generated which clears the main state flip-flops.

During the manual timing LM-3, the K-LA signal generates SREN. This signal enables the control panel switch register through an input multiplexer to the adder. The information that is set at the switch register under control of the console operator is then transferred through the adder and the second multiplexer onto the data bus, and directly into the data inputs of the four main registers in the computer. At the end of LT3 the PM3 pulse gated by the K-LA signal enables the PC LOAD pulse; this pulse will load into the PC register the information that is presented at its data input (Switch Register).

The computer memory is cycled during the time the load address key is operated, but the information displayed in the memory buffer register will correspond to the old address stored in the MAR register. The K-LA signal prevents the RUN flip-flop from being set at PT3 time. This inhibits the computer from running more than one cycle during the operation of the load address key.

If the load address key is pressed two consecutive times, the memory buffer register will display the data at the address specified by the switch register at the moment the load address key is pressed the second time. Circuitry is provided in the computer in order to prevent address zero from being loaded into the MAR if an interrupt request has been issued to the processor at the time that the load address key is pressed. (The ION flag is on.)

DEPOSIT KEY (K-DEP). This key allows the contents of the switch register to be stored in core memory at the address previously specified by the load address operation.

When the deposit key is pressed the K-DEP signal is issued to the processor from the front panel. This signal sets the STFF flip-flop that initiates the timing sequence of the computer. During LM1 time the MANPRES signal clears the main state flip-flops. During LM2 time the PC enable signal gates the PC register via the first multiplexer through the adder and enables all the signals to the data bus of the computer. At PM2 time the MAR Load timing pulse gates the content of the PC into the memory address register.

During LM3 time the MAREN-0511 and the MAREN-0004 signals are enabled. These two signals gate the MAR register into multiplexer A of the arithmetic section, and then to the bus. The CARRY IN signal is also enabled during LM3 time and this increments the contents of the memory address register by one. The PM3 timing pulse produces the PC LOAD signal that loads the contents of MAR into the PC.

The read portion of the memory cycle is initiated at LT1 time. During LT2 time the K-DEP signals inhibit the memory data from being applied into the input multiplexer. During this period the switch register is enabled into section A of the input multiplexer. The memory buffer register is then primed to accept data at PT2 time. This new information at the MBR is stored into the core memory during the write portion of the present memory cycle. This completes the transfer of information from the switch register to memory.

Subsequent data can be deposited in memory by setting the switch register and pressing the deposit switch. Every time that the deposit switch is pressed, the PC is incremented by one in order to specify the next memory address for the next deposit.

EXAMINE KEY (K-EX). The purpose of this key is to examine the contents of any memory location specified by the memory address register. The PC is also incremented by one every time that this key is operated in order to facilitate the inspection of consecutive memory locations. The timing operation of the PC and MAR are similar to the deposit key, but during the read portion of the memory cycle the section of the multiplexer that enables the data lines from the memory data register are enabled (LT2 Timing). The data from memory is then stored in the MBR register, and this is used for restoring the information back to memory during the write portion of the memory cycle. The K-EX signal also inhibits the RUNFF flip-flop from being set at PT3 time.

START KEY (K-ST). The operation of this switch initiates the execution of a program stored in core memory. When the start key is pressed, the K-ST signal is issued by the front panel to the computer. This signal sets the STFF flip-flop which in turn starts the timing generator. The MANPRES signal clears the computer state flip-flops during LM1 time. A clear signal is also produced which clears all the I/O devices connected to the external bus. The PAUSE flip-flop and the I/O shift register used for producing the IOP timing pulses are also reset.

During LM2 time the contents of the PC register are transferred to the memory address register as in a deposit or examine operation. During PM-3 time the ACCLOAD signal is produced. Zeroes are then loaded into the accumulator and link since the input multiplexer of the arithmetic section is not enabled at this time. This results in a clearing of the accumulator and link.

The START signal is produced by PM3 and K-ST timing signals. This signal presets the FETCH flip-flop which places the computer in that state.

During the FETCH state the PCSTEP signal is generated. This signal at LT1 time enables the

CARRY IN and the MAR into input multiplexer B. The timing pulse PT1 produces the PCLOAD command. This pulse loads the contents of the MAR register incremented by one into the program counter. These operations increment the PC during LT1 time of the FETCH cycle.

The RUN flip-flop is set at PT3 time. This allows the computer to execute any program stored in its memory. The RUN flip-flop enables the feedback loop of the timing chain to allow the timing pulses to be continuously generated.

STOP KEY (K-Stop). When this key is pressed by the operator, the computer is allowed to complete the instruction that is presently being executed. The RUN flip-flop is cleared at PT3 time of the last memory cycle. Once the RUN flip-flop is reset it inhibits the timing generator of the computer in state LT4 prior to PT4 time. The next time any of the control switches are pressed PT4 is generated. This allows different information to be shown in the PC and MAR registers. The PC has the address of the next instruction to be executed, and MAR the address of the last instruction executed. Pressing the start and stop keys at the same time allows the computer to execute a single instruction.

SINGLE STEP KEY (K-SSTEP). When the single step switch is activated, it prevents the setting of the run flip-flop at PT3 time. This allows the computer to execute instructions one cycle at a time, thereby allowing the operator to follow the different steps of the program. In order to implement several consecutive cycles the continue key should be pressed after the program is initiated by the start key. When the single step switch is pressed down, an indicator lamp on the control panel indicates that the computer is in a single step mode.

RESET KEY. When this Switch is pressed by the operator it produces in the computer the same power clear signal that is generated when the computer is turned on. The POWER CLEAR signals clear the timing shift register of the computer, the RUN flip-flop, the I/O PAUSE flip-flop, and issues a clear command to all the I/O devices connected at the I/O bus of the processor.

CONTINUE KEY (K-CONT). This key sets the RUN flip-flop at PT3 time and the processor starts to execute the program in its memory. The continue key inhibits the MANPRES signal. This prevents the altering of the state and information stored from the last computer cycle.

MEMORY PROTECT KEY. This key is activated when it is in the up position. Its function is to protect the information stored in the last page of memory. When more than 4K is used, the last page of the highest field is protected.

The memory protect key prevents the altering of the protected page through operator error or under program control. When new information is to be stored in that page, the memory protect key should be placed down and then restored after the program is stored in that page. The processor provides the circuits that are constantly checking the memory address register in order to detect the address of the last page of memory (7600-7777 octal). This circuit is enabled by the K-PROTECT signal from the control key at the operator's console and the EMA signal that is hard wired to the highest field.

Two other signals are used for controlling the operation of the memory protect key. They are MEMPROT-1 and MEMPROT-2. These signals are utilized to prevent depositing information and are active whether a manual deposit, a data break, or a programmed writing is required.

If either memory protect signals are active and the address being stored at the MAR corresponds to the last page of memory, the processor generates the MEMPROT signal during LT2 time. This signal sets the memory illegal reference flop and also inhibits the ACCEN logic signal that enables the accumulator if a DCA is being processed during the Execute cycle. The PC is also inhibited if a jump to subroutine is being processed during the execute cycle of the computer. The MEMPROT signal also inhibits the DATAEN and SREN signals if a data break or switch register transfer is taking place. Finally, the carry in is disabled if any incrementing is to occur in the adder.

The memory illegal reference flop when set produces the I-REF signal. This signal effects two circuits in the processor. The first prevents PC LOAD from changing the information in the PC if a jump to subroutine is being executed, the second resets the RUNFF at PT3 time stopping the operation of the computer. An indicator lamp is also operated by this I-REF signal indicating to the operator that violation of the memory protect field has been detected by the processor.

The control logic of the D-112 has a MANINHFF flop that is normally cleared when power is applied. This flop is set whenever the run flop requires setting at PT4 time. This flop is also reset whenever the RUN flip-flop is reset. Its function is to prevent any action by the operator (except stop, reset, and single step) from occurring while the program is being executed. The D-112 also provides a panel lock which allows the operator to inhibit all the control keys in the front panel of the computer. When the power lock is set to lock, all key functions of the computer are inhibited. The only switches active are the switch register, data field register and instruction field register.

4.0 THEORY OF OPERATION FOR DIFFERENT INSTRUCTIONS

The following paragraphs describe the operation during instruction execution.

Each time the start key is pressed the computer enters the FETCH state at the address specified by the PC register.

There are basically three types of instructions performed by the D-112. They are: memory reference instructions, operate instructions, and IOT instructions. The first 3 bits of the instruction word contain the operation code, bits 3 and 4 contain the information about the type of addressing being specified, and finally bits 5 through 11 supply the address. For the operate instructions a memory address is not required. These instructions manipulate the ACC of the computer. Bits 3 through 11 of the instruction specify the operations to be performed on the accumulator during the fetch cycle. The operate instruction has micro-programming capability, since several operations can be combined within a single instruction. Finally, the IOT instruction allows the computer to communicate with the peripheral devices connected to the I/O bus.

4.1 MEMORY REFERENCE INSTRUCTIONS

The D-112 Users Manual should be consulted for the detailed description of the Memory Reference Instruction. All Memory Reference Instructions, with the exception of JMP, enter the Fetch and Execute states to secure their direct address. Only the JMP instruction can utilize the Fetch state without also entering the execute state. For indirect addressing the Defer state is also used.

Following is a detailed description of the various steps necessary for the implementation of a Memory Reference Instruction. As an example the first instruction is detailed using both direct and indirect addressing. The rest of the instructions are described using direct addressing. The jump instruction is described using both direct and indirect addressing.

4.1.1 AND (OP Code 0)

This instruction performs the logical AND operation between the contents of the ACC and the contents of the Addressed Core Memory Location. The results of this operation are stored in the ACC. The original contents of the ACC are lost, and the information stored at the memory location remains unchanged.

A detailed sequence of events is listed below for the AND instruction.

a) The computer enters the FETCH state prior to the execution of any instruction. It is set when the start key is pressed, or at the completion of the last instruction performed. In this case the FETCH state is set at the leading edge of PT4.

b) In the Fetch state the signal PC STEP is enabled. This signal performs two main logic operations. First, during LT3, it enables the MAR register and CARRY IN signals. Secondly, it produces at PTl time the PC LOAD signal. This signal loads the contents of the memory address register incremented by one into the program counter. This operation is always performed during the Fetch cycle.

   PC STEP is also enabled by TY Cycle and EA Execute which are used for options.

c) A memory cycle is also started at LT1 time at the address specified by the MAR register.

d) At LT2 the contents of the memory data register, MEM, is enabled into multiplexer A and loaded at PT2 time. This timing pulse also loads MEM 0, 1, 2 into the instruction register.

   The contents of the instruction register are decoded in order to specify which instruction is to be executed. In this case the AND instruction is decoded.

e) During LT3 time no operation is performed in the computer for the AND, TAD, ISZ, DCA, JMS and JMP when indirect addressing is used.

f) During LT4 time, the address of the next memory cycle necessary for the EXECUTE or DEFER cycle is specified. It is formed by enabling the signal MEMENØ511, which enables into the input multiplexer bits 05 to 11 of the current instruction.

   The remainder of the address (bits 00 - 04) are enabled according to the information contained in the address control bits of the instruction register (bits 03 and 04). MBR03 = 0 means that the instruction uses direct addressing and the computer state goes to EXECUTE. MBRO3 = 1 means that the instruction uses indirect addressing and the next cycle to be executed by the computer is DEFER.

   If MBR04 = Ø no signal is enabled in the section 00-04 of the input multiplexer and the MAR register is loaded with zeros transferring into MAR ØØ through MAR04. This means that we are referring directly to page zero for addressing of the EXECUTE cycle.

   If MBR04 is equal to 1 signal MARENØØØ4 is enabled which enables bits ØØ to 04 of the MAR register which contain the page address of the current instruction.

g) During the last portion of the FETCH state, the memory of the computer completes the write cycle to restore the data to the current instruction fetched at the beginning of the cycle. MBR and MAR supply the data and the address to the memory during the restore operation.

h) At the leading edge of PT4 the EXECUTE cycle is set into the computer, if MBR03 = Ø (direct addressing).

i) A new memory cycle is started during the EXECUTE cycle. The address is specified by the MAR register, and the contents of the addressed memory location is stored into the MBR register at PT2 time.

j) The contents of the MBR register is then ANDed with the contents of the ACC register. The result of the AND operation is then applied to the output multiplexer and enabled during LT3 time. The ACC is then loaded at PT3 time, storing the result of the AND operation into the ACC.

k) During the second half of the EXECUTE state, the operand is restored to memory during the write portion of the memory cycle. The operand is unchanged during the AND process.

l) The PC is normally loaded into the MAR during LT4 if there is not a break request signal present. The FETCH cycle is also set in order to execute the following instruction after the AND operation. The program is then ready to fetch and execute the next instruction from the location specified by the MAR register.

m) If MBR03 is equal to 1 during the FETCH state of the AND instruction the computer enters the DEFER cycle instead of EXECUTE.

   The address stored in MAR for specifying the address of the memory cycle during the DEFER cycle, is formed by low order bits 05 through 11 of the AND instruction,

and could be either the address of the current page where the program is being executed or the address of page zero according to MBR04.

n) During the DEFER state at LT2 time the new indirect memory address where the operand is taken during the EXECUTE cycle is loaded into the MBR register.

o) During LT4 the new address stored in the Memory Data Register is transferred into the MAR register. This starts a new memory cycle for the EXECUTE state. If auto indexing is being used the signal AUTINDADD is enabled. This signal enables the CARRY IN signal into the adder, incrementing the address by one.

At PT4 time the control of the computer is transferred from DEFER to EXECUTE proceeding with the same sequency of events as previously described.

4.1.2 TAD (OP Code 1)

This instruction adds the contents of the ACC register with the contents of the specified memory address location. The addition is performed with 2's complement arithmetic, the result is stored in the ACC. The addend (operand) is restored unchanged into the memory.

The series of events during the FETCH cycle for the TAD instructions are similar to the AND instruction. The only difference is that the IR register stores and decodes the octal number 1.

Following this the processor executes either the DEFER or EXECUTE cycle according to the type of address being specified by the instruction. The first cycle is similar to that of the AND instruction. The following paragraphs describe a series of operations performed during the Execute cycle.

a) During LT2 time of the EXECUTE cycle the addend is stored in the MBR from the memory data register.

b) During LT3 time the ACC is enabled into multiplexer B and the memory data register MEM is also enabled into multiplexer A. Note that the contents of the MEM are used instead of the contents of the MBR register. The output of the adder is stored in the ACC at PT3 time.

The CARRY OUT signal produced by the adder is exclusively ORed with information stored in the LINK register, producing the ADD LINK signal. This signal is gated to the input of the LINK register and stored in it by the same signal that is used to load the ACC register. This provides the complementing operation of the LINK for the 2's complement arithmetic.

c) During the write portion of the memory cycle, the operand stored in the MBR is restored in its original memory location.

d) The LT4 portion of the FETCH cycle is similar to that of the AND instruction. The processor starts the next FETCH cycle if there is not a break request or interrupt awaiting service.

4.1.3 ISZ (OP Code 2)

This instruction provides a way to increment and check for overflow of the contents of the addressed memory location. The incremented contents of the MBR are restored into the same memory location. If the incremented contents are zero, an overflow signal is produced setting the SKIP flop in order to increment the contents of the PC register by one. This causes the program to skip the next instruction to be executed after the ISZ.

The sequence of steps to implement the execution of this instruction are as follows:

a) The FETCH state of this instruction is the same as the operation of the AND instruction. The only difference exists in the contents of the IR register which is loaded with the operation code 2.

b) During LT2 time the contents of the memory data register are stored through the adder into the MBR register. The CARRY IN signal is also enabled at the time of this transfer into the adder which adds one to the operand before it is stored in the MBR.

c) The input of the SKIP flop is enabled during this period by the CARRY OUT signal. This flip-flop is set if an overflow is produced and the CARRY OUT is equal to one.

d) During the Write portion of the memory cycle, the incremented operand stored in the MBR is restored into the same memory address location from which it was previously removed.

e) There is no operation for this instruction during LT3 time.

f) During LT4 if there is no break or interrupt request, the content of the PC is transferred into the MAR register. During this transfer the SKIP flip-flop (if one) enables the CARRY IN signal into the adder, incrementing the content of the PC at the time of the transfer into MAR. This operation produces a skip of the next instruction to be executed by the computer.

4.1.4 DCA (OP Code 3)

This instruction transfers the contents of the ACC register into the addressed memory location and then clears the ACC. The information previously stored in that location of memory is lost. The sequence of events performed for this instruction follows:

a) During the FETCH cycle this instruction executes the same series of events as the AND instruction. The only difference is that the IR register stores and decodes the Octal number 3.

b) In the EXECUTE cycle the MEMEM00 - 04,05 - 11 signal is inhibited. This operation prevents the contents of the memory data register from being transferred to the MBR.

During LT2, the signal ACCEN is enabled. This transfers the information stored in

the accumulator through the adder into the data bus. At PT2 time, the MBR is loaded with the information from the accumulator.

c) During the write portion of the memory cycle, the contents of the MBR is stored in the memory address location specified by the MAR register. This completely transfers the information from the accumulator to memory.

d) During LT3 all signals at the multiplexer are disabled and information on the data bus equals zero. The accumulator is then loaded at PT3 time, storing the contents of the data bus (zeros) in the ACC. This operation clears the accumulator.

During LT4 time, the series of operations performed during the AND instructions are repeated.

4.1.5 JMS (OP Code 4)

This instruction provides for a program branch into a sub-routine. The current contents of the PC are incremented by one and stored in the location specified by the JMS instruction. This is the first address of the sub-routine, and it is used to save the return address to the main program when the execution of the sub-routine is completed. This operation is performed by an indirect jump from the last instruction of the sub-routine or any intermediate exit that it could have.

The following paragraphs describe the series of steps necessary for the implementation of JMS instruction.

a) The operation during the FETCH cycle of this instruction is similar to the AND instruction. The only difference is that the information stored in the IR register is the octal number 4.

b) During LT1 of the execute cycle, the read portion of memory cycle is initiated.

c) During LT2 of the Execute cycle, the signal enabling the contents of the memory data register into the MBR register is inhibited. This prevents the contents of the addressed memory location from being stored in the MBR; hence its contents are lost.

d) Also during LT2 the contents of the PC are enabled into the input multiplexer A, and then loaded into the MBR register. If the SKIP flop is on, the CARRY IN signal is also enabled incrementing the contents of the PC before it is loaded into the MBR.

e) During the write portion of the memory cycle the contents of the MBR (PC) are stored in the addressed core memory location.

f) During LT3, the contents of the MAR register (starting address of the sub-routine) are enabled and transferred to the PC. At the same time that this transfer is taking place, the CARRY IN signal is enabled incrementing this address by one. The PC then contains the address of the next memory instruction to be executed following the starting address of the sub-routine.

g) During the final LT4 if there is no data break request or interrupt present, the processor sets the FETCH cycle and starts to the next instruction.

4.1.6 JMP (OP Code 5)

This instruction is used to branch from a program being executed to a new program not located consecutively in memory. It is also frequently used in such program loops as counting or awaiting a flag from an I/O device.

The JMP instruction does not use the EXECUTE cycle of the computer.

The following paragraphs describe the sequence of steps for a direct or indirectly addressed JMP instruction.

a) The initial steps during the timing LT1 and LT2 of the JMP Fetch cycle are similar to that performed during the AND instruction. The only difference is that the octal number 5 is stored and decoded by the IR register.

b) During LT3 the signal MEMENØ5 - 11 is enabled into Multiplexer B. This portion of the current instruction being executed specifies the lower order bits of address to which the jump is going to be made.

c) The contents of MBR04 selects the type of address being executed by the computer. If MBR04 = 0 the inputs to multiplexer B for bits 00 to 04 are disabled. This implements the jump to page zero. If MBR04 = 1 the signal MAREN 00 - 04 is enabled and this gates the address of the current page being executed into the multiplexer. This address is finally stored in the PC at PT3 time.

d) During LT4, the contents of the PC is loaded into the MAR register. This transfers the new address into the MAR register prior to the next instruction.

e) IF MBR03 = 1 indirect addressing is indicated. No operations occur during LT3.

f) During LT4 the indirect address for initiating the DEFER cycle is loaded into the MAR register. The DEFER cycle is set by the control logic and a new computer cycle is initiated.

g) No operation is executed during LT1 of the DEFER cycle.

h) During LT2, the memory data register is enabled into the Multiplexer and transferred to the MBR register. If an auto index register is referenced by the jump instruction, the CARRY IN signal is enabled and the contents of memory are incremented before being loaded into the MBR. An auto index occurs when indirect reference is made by an instruction referring to the memory address 10 - 17 (Octal) of page zero.

i) During LT3 the contents of the memory data register are enabled and transferred into the PC register. If an auto index is referenced, its contents are incremented by one.

j) During the Write portion of the memory cycle, the incremented content of the MBR is restored into memory.

k) During LT4 the content of the PC register is transferred into the MAR register in order to specify the address of the next processor cycle to be executed by the computer. This address is the starting address of the location where the jump instruction has transferred control. The processor executes this instruction if there is no break or interrupt request from the I/O section of the computer.

4.2 OPERATE INSTRUCTION (OPR OP Code 7)

The OPR group of instructions are divided into two groups, Group 1 (OPR 1) and Group 2 (OPR 2). The Group 1 is defined by a zero in bit 03 of that instruction. They perform such operations on the ACC and LINK as clearing, rotating left, rotating right, complementing and incrementing. Group 2 is designated by a one in bit 03 and zero in bit 11 of the instruction. This group provides the means for skipping the next instruction to be executed under certain conditions of the ACC and LINK (ex: ACC = Ø, ACC positive, etc.).

4.2.1 GROUP I

Following is a description of the instructions executed during the OPR 1 group.

NO OPERATION (NOP)

This instruction 7000 (Octal) does not change the contents of the ACC and LINK. MBR04 and MBR06 are equal to a zero in this instruction. The signal XORMBR-46 is enabled. It is the complement of the exclusive OR of these two MBR bits. XORMBR-46 is ANDed with the OP1 signal to enable the accumulator into multiplexer B and the adder. The NO SHIFT signal is also generated transferring the contents of the accumulator onto the data bus. Hence, the accumulator and the Link are loaded with their own information.

INCREMENT THE ACCUMULATOR (IAC)

a) This instruction, 7001 (Octal), increments the contents of the accumulator. MBR-11 of this instruction is the only bit in the operand equal to one. The ACC is enabled at the input to multiplexer B of the adder. The CARRY IN is also enabled in order to increment the contents of the accumulator. The ACC is loaded at PT3 time storing its own information incremented by one.

b) Rotate accumulator left (RAL). This instruction, 7004 (Octal), rotates the contents of the ACC and the link left by one. MBR-09 equal to a one indicates that the rotate left instruction is to be executed. MBR-10 = 0 indicates that the rotate operation is only one step. The contents of the Accumulator is enabled into the input multiplexer. The signal ADDBUSS00 contains the information of the accumulator bit 00. This signal is selected at the input of the link. The signal LEFTSHFT is asserted and enables the input of the output multiplexer of the adder, shifting the accumulator left by one.

At PT3 time the shifted contents of the accumulator are loaded into the accumulator and link. The content of the link is stored in ACC-11.

c) Rotate left twice (RTL). This instruction, 7006 (Octal), rotates left twice the contents of the accumulator and the link. MBR-10 equal to a one indicates that the DLEFTSHFT signal is asserted. This enables multiplexer B to rotate the contents of the accumulator and link two bits to the left.

d) Rotate Accumulator right (RAR). This instruction, 7010 (Octal), rotates the ACC and LINK right one place. MBR-08 equal to a one indicates a right shift. MBR-10 equal to a zero together with the previous signal enables the RIGHTSHFT signal. This controls the selection of the output multiplexer in order to enable the accumulator or LINK signals to be shifted one position to the right.

e) Rotate right twice (RTR). This instruction, 7012 (Octal), rotates two steps to the right the contents of the ACC and LINK. MBR-10 equal to a one causes the DRGHTSHFT signal to be asserted. This signal enables the control of the output multiplexer which rotates the accumulator and link two steps to the right.

f) Complement Link (CML). This instruction, 7020 (Octal), complements the contents of the link register. MBR07 equal to a one activates the $\overline{\text{LINK}}$-EN signal. This control signal enables the complement of the link register to appear at its input. At PT3 time this information is stored in the link, hence complementing its contents. The ACC-EN and ACC load signals are asserted, therefore preserving the contents of the ACC during the execution of this instruction.

g) Complement Accumulator (CMA). This instruction, 7040, complements the contents of the ACC. MBR06 equals one, and no other bits of the operand are set, causing the signal $\overline{\text{ACC}}$-EN to be asserted. This signal enables the complement of the accumulator into the input of multiplexer B. This information is transferred to the input of the ACC and loaded at PT3 time. The content of the LINK is also enabled into its input in order to save this information when both registers are loaded.

h) Complement and Increment the Accumulator (CIA). This instruction, 7041 (Octal), complements and increments the information stored in the ACC register. MBR06 equal to a one enables the $\overline{\text{ACC}}$-EN signal. This control signal enables the complement of the ACC into the multiplexer B. MBR-11 equal to a one enables the CARRY IN signal that increments the complement of the ACC when it is transferred through the adder. The ACC is loaded with the new information. The LINK is also enabled in order to save the information that is stored in it.

i) Clear Link (CLL). This instruction, 7100 (Octal), clears the information stored in the LINK register. The logic signal LINK-EN that is normally enabled during most of the OPR instructions is inhibited by MBR05 equal to a one. The Link then has its data input equal to zero and the load pulse then

clears the Link. The ACC is enabled to the input multiplexer of the adder in order to save the information that is stored in that register.

j) Set Link (STL). This instruction, 7120 (Octal), sets the LINK register to one. The LINK-IN and $\overline{\text{LINK}}$-EN are enabled at the same time, and their logical OR is supplied to the input of the LINK register. When the link is loaded it is then set to a one. The ACC is also enabled into the input multiplexer in order to preserve its information.

k) Clear the Accumulator (CLA). This instruction, 7200 (Octal), clears the contents of the ACC register. MBRØ4 equal to a one inhibits the accumulator from being enabled into multiplexer B. When the accumulator load signal is produced, the contents of the data bus are equal to zero, setting the contents of the ACC to zero. The contents of the link is also enabled into its input in order to preserve the information stored in it.

l) Set Accumulator (STA). This instruction, 7240 (Octal), sets the contents of the ACC equal to one. This operation is a logical combination of the CLA and CMA commands. The signals ACC-EN and ACC-EN are enabled at the same time at the input to the multiplexer B. The logical OR is supplied to the data bus at the input of the ACC. When the ACC is loaded all ones are transferred into this register. The contents of the link is also enabled in order to preserve the information stored in it.

4.2.2 GROUP II

This group is specified when MBR03 is equal to a one, and MBR11 is equal to a zero. This microinstruction may also be combined to give microprogramming capabilities.

There are seven steps that are executed in the same way for all the OPR 2 group of instructions. The operations performed during LT1 and LT2 of the FETCH cycle are similar to those of the OPR1 and the AND instruction already described. Following is a description of this group.

a) HALT (HLT). This instruction, 7402 (Octal), resets the RUN flip-flop at the end of LT3. This operation stops the computer from executing the next instruction during a normal RUN operation. The computer actually comes to a halt. MBR-10 equal to a one and MBR-11 equal to a zero produces the control signals necessary for resetting the RUN flip-flop.

b) OR with Switch Register (OSR). This instruction, 7404 (Octal), inclusive OR's the contents of the switch register with the contents of the accumulator. MBR09 equal to one, and MBR-11 equal to a zero are combined with the OP2 logic signal to assert SREN. This signal enables the switch register into multiplexer B of the adder. The ACC-EN signal is also asserted, thus the ACC and SR are both applied to the same multiplexer. This operation inclusively OR's the contents of both registers onto the data bus. This new information is loaded into the ACC. The contents of the LINK is also enabled into its input in order to preserve the link.

If MBR04 is equal to a one, the ACC-EN is inhibited. This allows only the switch register to access the data bus. This instruction is equivalent to loading the switch register into the ACC directly, and the information previously stored in the accumulator is lost.

c) Skip unconditionally (SKP). This instruction, 7410 (Octal), increments the contents of the PC, in order to skip the next instruction to be executed by the computer.

During PT3 time of an OPR group FETCH cycle a clock signal is present at the SKIP flop. The information to the input of the SKIP flip-flop is enabled according to Group 2 operating instructions.

For the skip instruction MBR08 equals a one, and no other bit of the operand is set. The data input to the SKIP flip-flop is enabled by MBR08 equal to a one, MBR-11 equal to a zero, and the OP2 signal. The SKIP flip-flop is set at PT3 time.

During LT4 the CARRY IN signal is enabled by the SKIP flop. This operation increments the contents of the PC register during the time it is transferred into the MAR register, in order to specify the address of the next instruction to be executed. This operation results in the skip of the next address.

d) Skip on Non-zero-Link (SNL). This instruction, 7420 (Octal), samples the contents of the link register. If it contains a one, the contents of the PC are incremented by one in order to skip the next instruction to be executed. MBR07 equal to a one and MBR08 equal to a zero enable the content of the LINK register into the input of the SKIP flop. The SKIP flop then is set if the LINK contains a one, also the PC information being transferred during LT4 is incremented by one when loaded into the MAR register.

e) Skip on Zero Link (SZL). This instruction, 7430 (Octal), senses the contents of the register and, if it contains a zero, sets the SKIP flop. The PC is then incremented by one at the time of transfer into the MAR register. This instruction is similar to the previous one, but the contents of the MBR08 equal a one. It complements the contents of the link before it is applied to the input of the SKIP flip-flop. The operation during the LT4 is the same as explained before.

f) Skip on Zero Accumulator (SZA). This instruction, 7440 (Octal), senses the contents of the ACC register and, if it contains a zero in all its bits, the SKIP flop is set. This is done in order to increment the contents of the PC at the time of its transfer into the MAR. The signal ACC-SKIP is a one only when all bits of the accumulator are zeros. This signal enables the SKIP flop if MBR06 equals a one and MBR08 equals a zero. At PT3 the clock

signal for the SKIP flop is produced setting it if the accumulator equals zero. The same operation occurs during LT4 as described before.

g) Skip on Non-Zero Accumulator (SNA). This instruction, 7450 (Octal), senses the contents of each bit of the ACC and, if any contains a one, the SKIP flop is set. This allows the contents of the PC at the time of transfer into the MAR register to be incremented by one. An SNA instruction is logically similar to the SZA described before. MBR08 equal to a one reverses the sense of the ACC SKIP signal. The ACC-SKIP signal initially equals zero. If any bit of the accumulator is equal to one, this signal is inverted under control of MBR08 and applied to the input of the SKIP flop. The SKIP flop is set at PT3 time. The same series of events as described before occurs during LT4.

h) Skip on Minus Accumulator (SMA). This instruction, 7500 (Octal) senses the contents of the most significant bit of the ACC (ACC 00). The input of the SKIP flop is enabled if MBRØ5 equals a one, MBRØ8 equals a zero and ACØØ equals a one. Under these conditions the SKIP flop is set at PT3 and the same set of steps occurs as during LT4 of the previous instructions.

i) Skip on Positive Accumulator (SPA). This instruction, 7510 (Octal), senses the contents of the most significant bit of the ACC, and if it contains a zero, the SKIP flop is set. This increments the contents of the PC again. This instruction is similar to the SMA already described, but the contents of MBR08 equal a one and the information coming from ACC00 is inverted before it is applied to the input of the SKIP flop. If ACC00 equals a zero, a logic one is applied to the SKIP flip-flop and the flop is set.

j) Clear Accumulator (CLA). This instruction, 7600 (Octal), loads all zeros into the ACC in a manner similar to that of the OP1 group. It allows the ACC to be cleared after any of the skip instructions, hence utilizing only one computer cycle. The CLA is also used to provide ways of loading the switch register directly into the accumulator without any OR operation with the accumulator (LAS).

Each time the SKIP flop is set, during any of the previous SKIP instructions, it is automatically reset by the PC LOAD signal.

This signal is always issued at PT1 time of the next instruction to be executed after the SKIP flop is set. The OPR 2 instructions can also be logically combined in order to provide the operation of more than one instruction at a time. The D-112 User Handbook should be consulted for a detailed description of these microprogramming facilities.

4.3 INPUT/OUTPUT TRANSFER INSTRUCTIONS (IOT, OP Code 6)

This instruction allows the processor to communicate with the internal and external devices connected to the I/O bus. The instruction under programmer control can generate three timing pulses (IOP's) used for timing, sequential control applications, synchronization, and data transfer functions of the peripheral devices.

There are two basic types of IOT instructions. The first one is called the long IOT instruction, (4.5 μsec) during which time the IOP pulses are generated. The IOT's are used by the processor to control peripheral devices connected to the Internal I/O bus or the External I/O bus. The other type is called a short IOT where no IOP pulses are issued. These IOT's are used by the processor to control options located in the mainframe of the computer, and a regular memory cycle is used for the length of this instruction (1.2 μsec).

Following is a description of a series of events for the implementation of the long IOT instructions.

a) During LT1 and LT2 of the IOT FETCH cycle, the Logic operations are identical to that of the AND instruction. The IR register stores and decodes number 6 (Octal) that corresponds to the IOT logic signal. This signal is used for the control of the IOP generator and some other processor functions.

b) The IOT level during the FETCH cycle enables the LONG CYCLE signal if none of the short IOT device addresses are being referenced. The LONG CYCLE signal enabled by the MASTER CLOCK timing pulse generates the IO START signal. This signal sets the PAUSE flip-flop.

c) During LT3, the pause flop stops the main timing generator of the computer in order to provide an expanded cycle for the generation of the IOP's. At the end of the LT3, the PAUSE flop triggers the IOP generator. The Shift signal is produced initially by the PAUSE at LT3. This clock triggers the IODEL one shot that controls the separation between IOP-1 and LT3. It also controls the separation between any two IOP's and between IOP4 and LT4. The SHIFT clock controls the shift register that produces the IOP pulses. The first bit of the shift register is enabled during PT2 time. If an I/O operation is not required, this bit is always cleared during LT4.

The first bit to be shifted into the shift register corresponds to BOUT which is necessary for the generation of the IOP1. The IODEL one shot after a delay of 300 nanoseconds triggers the IOWD one shot.

This controls the width of the IOP pulses (600 nanoseconds). During this time, if MBR11 is equal to a one, IOP1 is issued by the processor. At the end of the IOWD delay this one shot again produces the SHIFT clock. This clock shifts another bit into the COUT output for the generation of IOP2. This triggers the IODEL delay one shot. The process is repeated again for the generation of IOP2 if MBR1Ø is equal to one, and for IOP4 if MBR09 is equal to a one. Finally, EOUT from the shift register is set up generating the IOEND signal. This completes the sequence of the IOP generator. The IOEND signal

prevents the IOWD one shot from being triggered and the timing feed back loop is opened. The SYNC flip-flop is also set at this time in order to provide a synchronization of the computer timing generator with the end of the I/O cycle. The SYNC signal produced by this flip-flop sets the LT4 flip-flop under control of computers crystal clock. The IOEND signal also generates the PRIOEND signal that clears the PAUSE flip-flop. During LT4, the I/O shift register is also cleared.

d) Each time an IOP is produced, the IOCLK-CONT signal is enabled. This triggers the SIOCK one shot. The one shot produces a narrow clock signal IOCLOCK which is delayed 500 nanoseconds. This clock signal is used to sense the I/O skip line in order to set the SKIP flop under the peripheral device request. The I/O CLOCK also produces the ACC LOAD signal in order to store information in the accumulator from any I/O DEVICE during the IOT instructions.

e) The ACC is loaded whenever any I/O clock is issued by the computer. The I/O Enable signal gates the accumulator to multiplexer B of the adder if the I/O ACCLR signal is not asserted by the I/O device. This OR's the ACC with the information from the peripheral device. If the I/O ACCLR signal is asserted by the device at the time of the transfer, the ACC register is not enabled into the input multiplexer B and the transfer corresponds only to the information from the device.

f) An extended IOT is not generated for certain options such as Memory Extension, Interrupt Enable, and Teletype. The LONG CYCLE signal is not enabled and the PAUSE flop is not set. A regular computer cycle is then executed for the IOT. If there is any transfer of data between the option and the accumulator of the computer, the EXIOEN signal is asserted by the device and the I/O enable signal is generated. This signal is gated with the computer's internal timing, such as LT3. The ACC LOAD signal is generated by the external device and appears via the MEACCLD line.

g) During LT4, the same sequence of operations occurs as for the AND instruction. If the SKIP flop is set by any I/O device, the contents of the PC is incremented by one at the time of transfer into the MAR register.

4.4 INTERRUPT

The program interrupt facility in the processor allows the peripheral devices under certain conditions to interrupt the computer's execution of a program. When a peripheral device wants to interrupt the computer, it issues an interrupt request into the processor. When the processor answers the interrupt request from the device, it has the task of identifying which device is requesting service. This is carried out by the use of IOT instructions in conjunction with the SKIP facilities of the computer.

The programmer can control the interrupt facilities of the processor by direct setting of the INT INHIBIT flip-flop. This enables the processor to respond to an interrupt request. If the INT INHIBIT flip-flop is reset, the processor does not respond to an interrupt request from a peripheral device.

The set and reset of the INT INHIBIT flip-flop are controlled by two IOT instructions.

4.4.1 ION (6001, Octal).

This instruction enables the CPU IOT signal. This gated with the decode of MBR-10 or MBR-11 enables the clock to the INT INHIBIT flip-flop. If MBR-11 equals a one, the interrupt inhibit flip-flop is set. The interrupt inhibit flip-flop also controls the INT ENABLE flop. This flop provides the delay of one cycle after the inhibit flip-flop is set. This allows the programmer to jump out of the interrupt handling sub-routine when an interrupt request is being processed. (For reference, the D-112 User's Handbook should be consulted.) The INT ENABLE flop clock is set at the leading edge of LT4 of the cycle following the setting of the interrupt inhibit flop. Once the INT ENABLE flop is set, the processor is prepared to answer an interrupt request from any peripheral device.

4.4.2 IOF (6002, Octal)

This instruction resets the INT INHIBIT flip-flop in cases where the programmer does not want the processor to be interrupted by a device. MBR11 clears the interrupt flop at the time that its clock is being issued.

The following paragraphs describe the series of steps in the processor, after it has answered an interrupt request from any peripheral device.

a) When any peripheral device sets an interrupt request, the INTREQ signal is enabled. This signal is also ANDed with INTEN and produces a priority signal when the data break facility of the computer is being sensed. This occurs twice during a long IOT cycle (see data break description).

   The processor answers the interrupt request at the end of the execution of its current instruction. For example, during a three cycle instruction, the processor answers the interrupt request at the end of the EXECUTE cycle. The FSET signal is asserted when the next cycle is to be a FETCH state. The INTREQ flop is set at the leading edge of LT4 in order to answer the interrupt request from the device. This flop sets the INT signal which in turn controls the series of steps necessary for the interrupt implementation.

b) The INT signal sets the state generator of the processor to EXECUTE at PT4. It also sets the IR register to store the binary number 4, an equivalent JMS instruction. Finally, it inhibits any information into the multiplexer of the adder, and loads the MAR with all zeros. This forces location zero to be addressed.

c) If Memory Extension is utilized, the contents of the data field register and instruction field register are saved and the address of field zero is decoded by control.

d) The previous set of steps appear to the processor as a jump to a sub-routine at

location zero. During the forced EXECUTE cycle the contents of the PC register are stored in location zero. This saves the return address of the program to be used after servicing of the interrupt request.

e) The series of steps during the EXECUTE cycle are similar to those described for the JMS instructions. This implies that the next instruction to be executed by the processor is stored at memory location 1.

f) The INT INHIBIT flop is reset at PT1. This operation automatically inhibits the processor from answering any new interrupt request during the time that the interrupt is being serviced. The ION and IOF instructions are used by the programmer in order to operate on the interrupt inhibit flip-flop.

g) Finally, the INT INHIBIT flop is provided with a direct set and clear signal EXINTCLR and EXINSET in order to provide direct control from any peripheral device under customer's control.

h) The signal INTCONT is provided to externally inhibit the processor from answering an interrupt request. Typically it relates to the memory extension and control. The interrupt request from the processor can be disabled for a period of time, allowing critical instructions to be executed. For more details, the memory extension and control description should be consulted.

4.5 DATA BREAK

This option allows peripheral equipment connected to the data break facility to temporarily suspend the execution of the program in the computer, and transfer blocks of information to or from memory. The Data Break transfer does not involve program execution, and the contents of the PC, ACC, and the instruction register are not changed. After the transfer has taken place, the computer continues to execute the interrupted program.

The processor has in its control circuitry three main states assigned to the data break facility. They are DATA WORD COUNT, DATA CURRENT ADDRESS, and DIRECT DATA TRANSFER. There are two types of data breaks, single cycle and three cycle. The three cycle data break uses the three states of the computer already described. The single cycle data break uses only the direct data transfers (Data Break) in order to transfer information. For a more detailed description of each data break cycle the D-112 User's Manual should be consulted.

Following is a description of the data break states of the computer.

The peripheral device connected to the data break facilities of the computer has to request from the processor a break cycle. The request is the BRKRQST signal. This signal is sensed at PT1 time during each computer cycle. If there is a break request, the break start flop is set at this time. A double sensing of the data break request is supplied as an option for devices where a fast response is required. This double sensing is utilized during long IOT cycles. At this time the IOEND signals is ANDed with LONG CYCLE in order to provide a second sense during this instruction. In order to avoid signal races the DBK double sensing is given priorities over the interrupt request on the line.

Once the break start flop is set, the control logic waits until the computer finishes executing the current instruction. This time is distinguished by the assertion of the FSET signal. The signal BREAKOK is enabled, setting the control logic to the special state according to the selection of the peripheral device. The BREAKOK signal is gated with the THREE CYCLE selection signal. When this signal is asserted (high) the signal DWC is enabled and the data word count flop is set. This occurs in a three cycle data break. If the THREE CYCLE signal is not enabled (ground), the signal DDCSET is enabled. This signal sets the direct data transfer flop that allows entrance to the data break state. The BREAK START flop is reset by PT1 when the break request signal is disabled. The BREAK START flop is reset by PT1 when the break request signal is disabled. The BREAK OK signal also sets the ADD ACCEPTED flip-flop at PT4 time. This flop enables the ADD ACCEPT signal to the peripheral device notifying it that its request has been accepted. The ADD ACCEPTED flop is cleared by the next PT1 pulse.

4.5.1 Data Word Count (WC)

This state is entered when a peripheral device requires a three-cycle data break. The DWC flop is set and the computer executes one memory cycle in order to implement the word count. During LT4 of the previous memory cycle prior to entering the word count state the signal BREAKOK enables the DATADDEN signal. This signal enables the address for the word count cycle which is supplied by the peripheral device to be gated to the MAR in Multiplexer A of the adder. This operation allows the device to specify the address in core memory where the word count cycle is referred. The DWC signal also enables the CARRY IN to the adder. This allows the contents of the addressed memory location to be incremented by one at the time of transfer from the memory data register into the MBR register (LT2). This operation increments the contents of the word count address by one. When this incrementation is taking place (PT2), the CARRY OUT signal from the adder is enabled by DWC into the D input of the WCOVERFLOW flop. This flop sets if the CARRY OUT signal is asserted, indicating that the desired quantity of data transfers have been accomplished at the end of the current data break. The processor sends to the device the WCOVERF signal to indicate completion of the transfer. During the last portion of the memory cycle, the contents of the word count address are stored into memory. The DWC signal sets the input of the Address Accepted flop at PT4 time.

During LT4, the DWC signal enables MAREN 0004-0511 signal. This signal enables the contents of the MAR into the multiplexer of the adder and transfers its contents incremented by one back to the MAR. This operation stores in the MAR the address of the location following the word count address. This location specifies the memory address for the current address cycle which follows.

4.5.2 Data Current Address (CA)

The second cycle of a three cycle data break supplies the address of the memory location where the transfers of information take place. The address of the current address cycle, as explained previously, corresponds to the next memory location

after the word count cycle. During LT2 the contents of the current address memory location incremented by one are stored in the MBR. The CARRY IN signal is enabled during this time in order to effect the incrementation. If the signal BCAINCR is disabled by the peripheral device at the time of transfer, the CARRY IN is disabled. The word read during this cycle is not incremented and it is restored unchanged in memory during the last portion of the write cycle.

4.5.3 Direct Data Transfer (Data Break)

This cycle occurs when the data transfer takes place from or to the peripheral device. This state can be entered directly in one cycle data transfer or can be set after the data current address. The address in memory for the transfer of information is specified directly by the peripheral device in one-cycle data break. In three-cycle breaks the data current address cycle specifies it. The information is stored in the MBR at the beginning of the data break cycle. The direct data transfer flop enables the DDC signal. This signal ANDed with the BDATAIN signal (if a one, direction of transfer of data is to the processor) enables the MEMPROT1 signal. This inhibits the signal MEMEN0005 at LT2. This disables the memory data register from the input multiplexer during the read portion of the memory cycles. The data being read from memory is lost. During LT2 the DDC and BDATAIN signals enable the DATAEN. This allows the data supplied by the peripheral device to be stored in the MBR at PT2 time. The data is stored in memory during the write portion of the memory cycle, completing the transfer of information from the device to the computer. If BDATAIN signal is low (transfers from the processor to the device), the DATEN is inhibited and the memory data register is enabled into the input multiplexer. This operation allows the information stored in memory to be transferred into the MBR. The MBR output is supplied to the peripheral device. The data in the MBR is restored to memory during the write portion of the memory cycle. The break cycle can also be used as a memory incrementing cycle (see D-112 User's Handbook for detailed information). This option provides a way to increment the contents of the addressed memory location in order to count I/O events. The direction of transfer should be asserted from the processor to the device. The signal BDKMEMINC should be asserted by the peripheral device. This signal enables the CARRY IN signal at LT2. The CARRY IN increments the contents of the memory location at the time it is being transferred into the MBR, and is restored to memory during the write portion of the memory cycle. During the time the incrementing is taking place the CARRY OUT of the adder is enabled into the WCOVERFLOW flop to allow its setting if an overflow of the contents of the incremented location occurs. The signal WCOVERF is enabled if an overflow is sensed by the flop. This flop is reset at PT2 time of the next memory cycle of the processor.

If no other data break cycles are required, the FETCH cycle of the next instruction is executed at PT4 time of the data break cycle. The processor starts to execute sequentially the interrupted program.

5.0 PCB CONFIGURATION

The D-112 minicomputer hardware is implemented on five basic printed circuit boards. Two of these printed circuit boards house the processor, another PCB corresponds to the I/O interface, another the timing and control of up to 32K of memory and, finally, one printed circuit board for 4K of core. The memory of the computer is expandable in modules of 4K up to 32K with one PCB per 4K of core.

The processor boards are named CU-1 and CU-2. Both boards have approximately 100 integrated circuits including medium scale integration devices (MSI).

The CU-1 PCB contains the arithmetic section, the adder, the input and output multiplexer's, the decode section for controlling the input of the multiplexer, and the four main registers of the processor (ACC, MBR, MAR, and PC), the link, the interrupt, and finally the drivers for buffering all registers going to the PCB connector board.

The CU-2 PCB contains the timing generator of the processor, the crystal clock, the memory timing interface, the IOP generator, the instruction register and the decode, the SKIP flip-flop and its control, and all the control signals for the four main registers of the processor. The board also contains drivers for buffering all the signals going out of the printed circuit board to the connector panel. The physical location of the boards is shown in Fig. 1-1.

The I/O interface board contains all the drivers and receivers for the I/O bus plus the teletype interface circuitry. This board also contains the data break interface circuits.

The memory boards are described in detail in Section III. For any core configuration up to the maximum of 32K, only one memory timing and control board is required. For more than 4K of memory it is necessary to use the memory and extension control board in order to implement the extra address bits necessary for referencing all 32K of memory. Section VII should be consulted for the description of this option.

The D-112 minicomputer provides a position in its connector board for the extended arithmetic option. This option provides the hardware for multiplying and dividing. A position is provided at the top of the connector board to accommodate a Universal Board for implementing special options and/or controller interfaces.

SECTION III

CORE MEMORY SYSTEM

1.0 GENERAL

This section contains operating and maintenance information for the Core Memory System. This section is divided into four parts, Description, Theory of Operation, Maintenance, and Drawings.

2.0 DESCRIPTION

The D-112 has a basic configuration of 4096 (12-bit) words of core memory referred to usually as "4K". The memory capacity of the computer can be increased in 4K modules up to 32K. These modules are PC boards which are inserted into slots 9 thru 15 in the mainframe of the computer. (See Figure 1-1 in Section I)

When more than 4K of memory is used in the computer, it is necessary to use the MC-1 memory extension control. This PC board is inserted into slot 6 in the mainframe of the computer.

2.1 FUNCTIONAL

For the D-112 basic 4K core memory two PC boards are required. One board is called Timing and Control, the other is called the stack module (MM-1). Expansion is accomplished by adding a stack module for each additional 4K (plus an "EX-MEM" PC board). The timing and control PCB can drive up to 8 stack modules. Thus, a total of ten printed circuit boards are required for the 32K memory.

The interface between the processor and the memory is carried out by a data and address bus, plus timing signals. Twelve lines carry the address selected from the MAR to specify the word being selected. Another twelve lines carry the data to be stored during the write portion of the memory cycle from the MBR.

The memory supplies the processor with information during the read portion of its cycle.

The timing interface between the processor and the memory is controlled by two commands, the read and write commands. These pulses initiate the read/write operation of the memory. Once the processor sends an initiate command, the memory executes the cycle asynchronously, controlled by its own interval timing. The memory access time is approximately 350 nanoseconds.

All memory cycles (read/restore or read/modify/write) are executed in 1.2 microseconds. This time is controlled by the crystal clock and timing generator of the processor. Figure 3-1 shows a detailed timing diagram of the interface between the memory and the processor.

The timing signals are received from the processor by the Memory Timing and Control PC board which generates the necessary signals for the operation of the stack module. When the read timing pulse that is issued by the processor reaches the timing and control board it triggers the START "one-shot." The pulse produced by this "one-shot" produces two initiate clear signals called DRR0 and DRR1. The two signals clear the memory register to allow it to load data during the read cycle. The leading edge of the START pulse initiates the read timing "one-shot." The "one-shot" controls the width of the read timing pulse. The strobe delay "one-shot" is also triggered by the leading edge of the START signal. The one shot provides a delay required to initiate the leading edge of the sense strobe. The sense strobe width is established by the SENSE strobe width one-shot. The one-shot is triggered by the sense strobe delay one-shot. This insures that the core output is sampled at the optimum time. The output of the sense amplifiers indicates a one with a pulse and a zero by the absence of a pulse. This pulse sets the memory data register with the information read from memory. Data remains in the memory data register during the entire memory cycle.

A write initiate pulse coming from the processor triggers the EDC one shot. The clear signals produced by the width one shot is inhibited by the writing pulse thus saving the information stored in the memory data register during the previous read cycle. The start pulse also triggers the INHIBIT TIMING one shot. This one shot produces the inhibit timing that drives the inhibit drives. The leading edge of the inhibit pulse, through a delay, triggers the R/W TIMING one shot that produces the write timing pulse. The read timing and the sense strobe pulses are inhibited during the write operation.

The remainder of the memory timing and control board is the memory data register. This register is a 12-bit register that stores the information from the sense amplifier during the read portion of the memory cycle. The MTC board provides buffering to the data signals from the MBR, through inverters before going to the inhibit drivers located on the stack board.

The MTC board also provides buffering for the address lines from the processor. These buffers drive the line decoders on the stack board.

Test points are available to gain access to these signals for trouble shooting and maintenance. The memory timing and control logic diagrams indicate the location of these points.

The inhibit resistors are mounted on the computer panel printed circuit board located toward the rear of the computer. Locating these resistors at this point provides greater cooling for the power dissipated, and thereby improves reliability as well as stability of the memory system.

The Memory Stack board contains the address decoding circuits, line drivers, inhibit drivers, sense amplifiers, and core assembly.

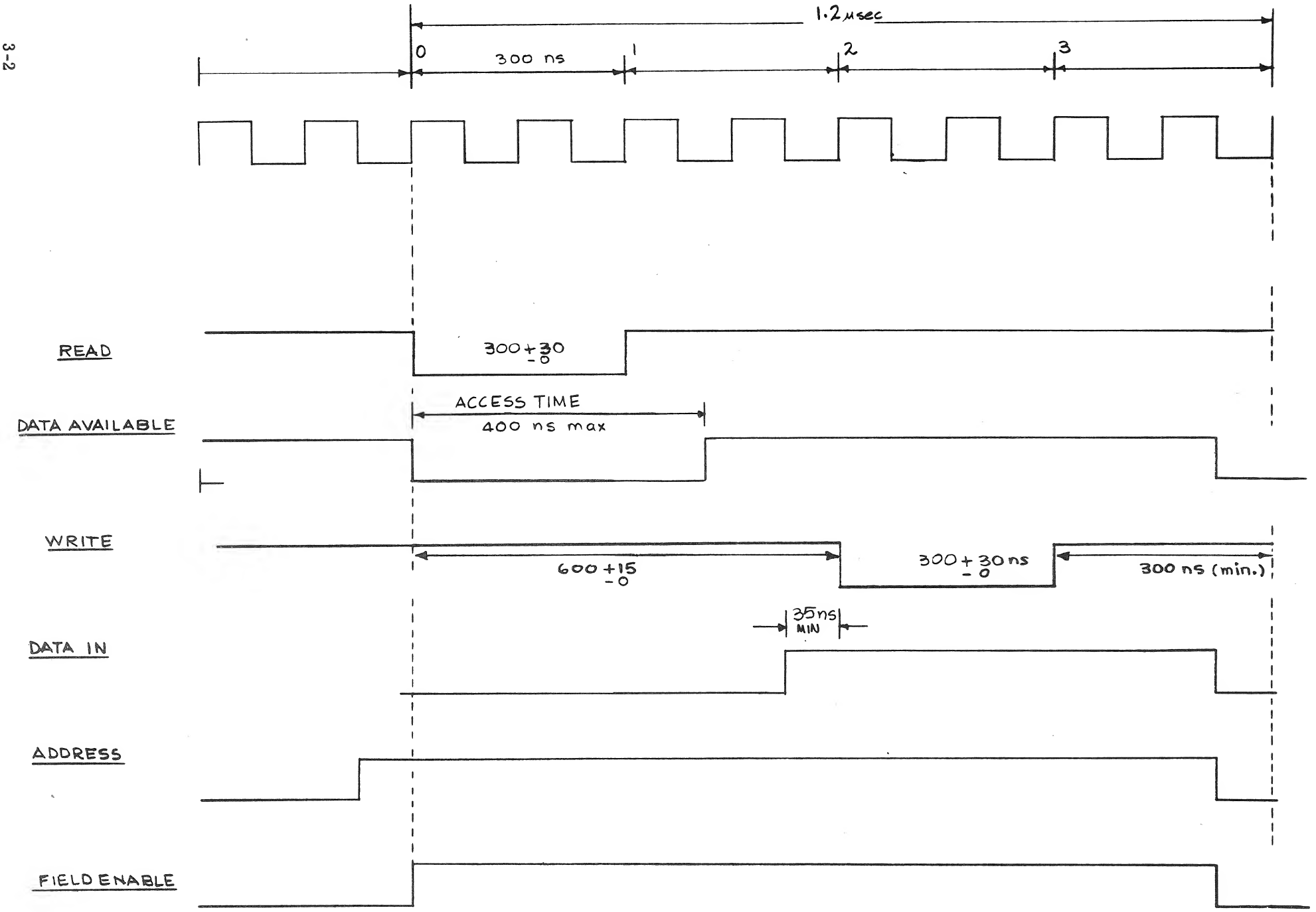


Figure 3-1. External Memory Signal Timing

The address decoders determine which line drivers are selected and thereby the X and Y lines to be activated. The drivers are controlled by the pre-drivers that essentially are read/write gates controlling the timing and direction of the current flow in the line drivers. These pre-drivers are enabled by the read and write command from the processor gated with the STACK SELECT signal that controls the stack selected by the processor when more than 4K of memory is being used. This signal, called field select, is supplied by a decode circuit provided in the Memory Extension and Control.

The inputs of the address decoders are supplied by the MA register from the processor. Each group of three input lines are connected to a binary-to-octal decoder that divides the 12-bit binary address in groups of three bits. Each binary group is decoded into one of eight possible discrete outputs to activate one gate. The active gates enable the selected line driver during any operating cycle. In order to complete the selection of one X drive line and one Y drive line, it is necessary to operate 4 gates, two for X and two for Y.

The memory system is organized around a three-dimensional, coincident-current magnetic-core stack which has three wires per core. Memory capacity is 4096-words of 12 bits per stack. Additionally, the basic memory can be expanded to a maximum of eight stacks. This gives a system capacity of 32,768 words in 4096 word increments.

Memory words are randomly accessible with a 15-bit address word from the processor. Maximum access time is 0.35 microsecond. The read/restore modes are implemented in a full memory cycle which is accomplished in 1.2 microseconds.

2.2 PHYSICAL

The basic core memory system consists of two printed circuit boards: the timing and control, and the stack board. The stack board has the core stack assembly mounted on it, secured by pin and socket connections. The core array within the core stack assembly is protected from handling damage by a removable hard cover.

Expansion of the memory system from the basic two-board configuration is accomplished by adding stack boards as necessary. Input/output connections for the memory are implemented with the two 86-pin edge connectors on the timing and control board. Memory system board interconnection is accomplished by wiring between the edge-connector sockets.

2.3 SPECIFICATIONS

Refer to Table 3-1 for a summary of system performance, electrical, environmental, and physical specifications.

Table 3-1. Specifications

Characteristics	Specification
PERFORMANCE:	
Memory Capacity	Maximum of 32,768 words of 12 bits each word.
Operating Mode	Read/Write
Access Time	0.35 microsecond max.
Cycle Time	1.2 microsecond cycle.
Access Mode	Random.
ELECTRICAL:	
Power Input Requirement	+12 VDC, ± 2% -12 VDC, ± 2% + 5 VDC, ± 5% (For current requirements, refer to Section 2.)
Logic Type	Standard DTL and TTL integrated circuits.
Logic Levels (worst case):	
Input	0 to +0.6 V low, +2.2 to +5.5 V high
Output	0 to 0.6 V low, +2.2 to 5.2 V high

Table 3-1. Specifications (Continued)

Characteristics	Specification
OPERATING ENVIRONMENT:	
Ambient Temperature Range:	0°C to 60°C
Humidity	To 95% relative without condensation.
Altitude limits	Sea level to 10,000 feet.
NON-OPERATING ENVIRONMENT:	
Ambient Temperature Range:	-30°C to +85°C
Humidity	To 95% relative without condensation.
Altitude limits	Sea level to 30,000 feet.
Shock and Vibration	Commensurate with normal commercial shipping.
Board Dimensions	15.995 in. x 12.995 in.
Memory Organization	3-wire, 3-dimensional array of 20-mil lithium cores on a single-sided matrix frame.

3.0 THEORY OF OPERATION

3.1 GENERAL

This section contains a functional description of the standard memory system at the block diagram level, and a detailed logic theory description. The logic diagrams referenced in the text are drawings no. 400051 and 400056 which are located in Volume II of this manual.

3.2 BLOCK DIAGRAM DESCRIPTION

Refer to the block diagram of Figure 1-2. This diagram includes a basic block diagram of the memory system. The system logic is divided into two main sections: the timing and control board, and the stack module board. The timing and control board receives address bits, control commands, and data from the external processor. The stack board is slaved to the timing and control board.

3.2.1 Timing and Control Functions

The timing and control logic sets initial conditions for the cycle and generates the required strobes and timing pulses to implement the data cycle. The data cycle is started by the read (READ) command. As soon as this command is received, a memory data register clear signal is generated (MDRCLO) to initialize the data register (MDR).

The data registers store the data read from core during the read portion of the cycle.

The address lines are buffered to present a single load to the external circuitry and increase the noise immunity of the system.

The inhibit drive current resistors, mounted external to the memory system, furnish the required amount of inhibit drive current to the inhibit drivers on the stack board.

3.2.2 Core Stack Functions

The stack board contains the core array (stack) and core line drive matrix logic. Each board installed is individually addressed by a line from the memory extension control board in the computer. The stack cores are then accessed by the X-Y drive matrix as a function of the core location portion of the address registers.

The stack cores are accessed by current coincidence on the X-Y drive line array. A third wire, the sense/inhibit line, recovers the core contents (sense) or writes data from the data registers to core (inhibit). Timing for the read and write operations is furnished by the timing and control logic (READ TIMING and WRITE TIMING), as is the INHIBIT TIMING for the write function.

The sense amplifiers recover data from the cores as a function of the current on the sense lines during READ TIME. The data available at the sense amplifier inputs is strobed to the data registers for output by the sense amplifier strobe from the timing and control board.

3.3 MEMORY TIMING AND CONTROL BOARD 400050 (PCB-7)

The timing and control board generates read/write timing signals and data address strobes. It also contains storage registers used to buffer data and the address words buffers. The descriptions of the logic in the following paragraphs should be used in conjunction with the memory system timing diagram, Figure 3-1, and Figure 3-3 which shows the drive current waveforms.

3.3.1 Data Register Control Gates

At the start of the cycle, the output of gate Z8-11 goes true and triggers the INITIATE one shot to generate the data register reset and strobe gates.

In the read/restore mode, the false Z3-6 and Z3-8 gate outputs generate data register reset MDRCLRO and MDRCLRY. These signals reset the data registers in preparation for receiving the core output.

3.3.2 Read/Write Timing

This logic is composed of read/write control gates Z1-6, Z1-8 and Z5-6; read/write timing gates Z8-3 and Z8-6; the R/W TIMING one-shot; and the INHIBIT TIMING one-shot.

Read control gate Z1-6 is used to control the start of the read/restore timing cycle. Read/write control gate Z1-8 is used to control the start of the read/write timing cycle during the read/write mode. Otherwise, both gates operate identically.

The output of the R/W TIMING one-shot at Z11-6 is applied to pin 5 of NOR-Gate Z5-6. This effectively stretches the width of the INITIATE pulse, which is still up at this time. The stretched output is applied to the core stack through read timing gate Z8-3, three inverters, and connector P1-B25. The positive READ TIMING pulse supplies the core read current.

The complement of READ TIMING is returned at inverter Z6-8 to the input logic of the INHIBIT TIMING one-shot. After a delay of 100 nanoseconds the complement of READ TIMING triggers the INHIBIT TIMING one-shot and sets the trigger input latch (Z10-3 and Z10-11). The latch prevents any subsequent read commands from retriggering the one-shot during a write cycle. The negative-going output of the INHIBIT TIMING one-shot at Z14-6 furnishes the INHIBIT TIMING current for the core stack through Z9-6, Z10-6, and P1-B36.

The positive-going output of the INHIBIT TIMING one-shot at Z14-8 enables write timing gate Z8-6. This gate is disabled, however, by the now negative level at the output NOR-Gate Z5-6. As the INHIBIT TIMING one-shot output goes negative at Z14-6, however, it supplies a delayed trigger to the R/W TIMING one-shot to start the WRITE TIMING period. The delay is injected by C4 to allow the inhibit current to rise to maximum prior to turning on the WRITE TIMING current. About 400 nanoseconds after the INHIBIT TIMING one-shot is triggered, the R/W TIMING one-shot is again triggered through gate Z5-6 to start the WRITE TIMING pulse. In addition to forming the WRITE TIMING pulse, the output of write timing gate Z8-6 is fed back to the INHIBIT TIMING one-shot trigger latch to reset the latch and allow operation on the next read command.

3.3.3 Data Read Logic (Sheet 2)

The data read logic is composed of the SENSE STROBE DELAY one-shot and the SENSE STROBE WIDTH one-shot.

The two one-shots provide the necessary delay and width for the sense amplifier strobe. At the start of a read operation, the WRITE (not) LEVEL provides an enabling signal to pin 3 of the SENSE STROBE one-shot trigger gate. As described in paragraph 3.3.2 the INITIATE pulse causes data register reset gates to produce data register reset signals MDRCLRO and MDRCLRY. They reset the data registers preparing them to receive data.

As the read current is turned on, the leading edge of READ TIMING from Z6-8 triggers the SENSE STROBE DELAY one-shot. After a delay of 350 nanoseconds, the level at Z12-6 goes true to trigger the SENSE STROBE WIDTH one-shot. The resulting 100-nanosecond pulse at Z13-8 is used in the stack to strobe the core output.

3.3.4 Data Registers (Sheet 2)

The two data registers are composed of 12 D-latches (Z22-5/9 through Z29-9 and Z30-5/9). During read, data from core (sense amplifier inputs) is direct set into the latches. Since the data is only capable of being direct set (nonreset facility for ZERO bits), the registers must be reset prior to reading core data. The reset is performed by MDRCLRO and MDRCLR1, as described in paragraph 3.3.2. In the read/restore mode, data is restored to core by the INHIBIT DRIVE BIT outputs. The read outputs are transferred to external equipment in the form of the DATA OUTPUT bits.

During write, data from the processor is present at the DATA INPUT (BUMBR). The input data is then written to core by the INHIBIT DRIVE BIT outputs.

The INHIBIT DRIVE currents are generated directly from the DATA INPUT lines through an inverting buffer driver.

3.3.5 Address Lines

The buffered Address Lines AL 00 through AL 11 are used to address core locations. Stack selection is effected by decoding which is accomplished on the memory extension and control PCB. The memory extension generates eight stack select lines which are used to specify stack on which the addressed core memory word is located.

3.3.6 Inhibit Resistors (Mounted External to the Memory System)

The inhibit resistors supply the inhibit current from the 12-volt supply to the selected stack board inhibit drivers. The inhibit current path during write is described in paragraph 3.4.2.

3.4 STACK BOARD

The stack board performs current sensing, inhibit current control, and X-Y drive current switching.

3.4.1 Sense Amplifiers

The 12 sense amplifiers perform the current sensing function for the maximum of 12 bits per data word in core. Since the operation of each amplifier is identical, the operation of Z24-12 is described here as typical.

Note that, since this memory system is a three-wire system, a common wire is used for the sensing and inhibit function; that is, the wire is used for sensing current during read and for conducting inhibit current during write. The common sense/inhibit wire is split into two lines within the stack so that one line is threaded through 2,048 cores of a 4096 core stack.

Sensing current from the sense/inhibit lines in the selected stack is applied to sense input lines SAO and SBO and the sense signal is developed across the differential amplifier input. Diodes CR128 and CR129 remain back biased since the signal is not large enough to forward bias them. At sense amplifier strobe time, the sense amplifier is strobed to transfer SENSE AMP OUTPUT 0 to the data register. Generation of the sense strobe is described in paragraph 3.3.5.

Application of the sense strobe is controlled through gates Z27-10 and Z27-12. These gates are enabled by the STACK SELECT signal. STACK select is the decoded line that is assigned to the particular stack board.

3.4.2 Inhibit Circuits

The inhibit drivers are selectively switched, transformer-coupled current sources. They switch inhibit current to the common sense/inhibit lines during the write portion of a cycle, depending on the logic level present on the data input lines (BUMBR). All 12 circuits are identical, therefore the circuit for bit 0 is described here as typical. Refer to Figure 3-2 for a diagram of a typical inhibit current loop.

Inhibit current from an inhibit resistor mounted on the computer Mother board is applied to isolation diode CR113. This turns on inhibit driver Q85 at INHIBIT TIMING time. The generation of INHIBIT TIMING is described in paragraph 3.3.4.

The inhibit driver passes the inhibit current to the common sense/inhibit lines in the stack. The inhibit current then is applied to SENSE LINE INPUT SA0 and SB1. The current level is sufficiently high to forward bias CR128 and CR129, which completes the current path to ground. (The sense amplifier remains unaffected since its input is returned to ground also through the diodes.)

3.4.3 X-Y Drive Circuits (Sheet 1)

These circuits are grouped as follows:

X SINK
Y SINK
Y WRITE DRIVE
Y READ DRIVE
X WRITE DRIVE
X READ DRIVE

Under control of four core location decoders and four X-Y read/write control gates, the groups form a 64 x 64 core driving matrix.

The control gating is composed of Z3-3, Z3-8, Z3-11, and Z3-6. The gates are enabled only when STACK SELECT from the Memory Extension and Control Board is true to select the particular stack board. At READ TIMING or WRITE TIMING, as described in paragraph 3.3.2, the gates select the read/write sink and drive the 8 groups as follows:

Z3-3: X-Y READ SINK at READ TIMING

Z3-11: X-Y READ DRIVE at READ TIMING

Z3-8: X-Y WRITE SINK at WRITE TIMING

Z3-6: X-Y WRITE DRIVE at WRITE TIMING

The specific X-Y lines within the group are selected as a function of the decoded lines from Z1, Z2, Z4, and Z5.

The following is the read switching current path for Y sink bit YS0, which is typical for all bit switches. Gate Z3-3 is enabled by READ TIMING and STACK SELECT. The output of the gate goes false to turn on pre-drive transistor Q17 through Balun transformer T5. At the same time, bits AL3, AL4, and AL5 from the address register are decoded to define bit 0 cores; consequently, decoder Z2-1 goes to ground. This provides a switching current path from ground, through the primary of T6 (read section pins 14 and 3), isolation diode CR26, current-limiting resistor R11, the collector of Q17, to +12V. Thus, one-half of the read sink current has been supplied to 64 bit 0 cores on the selected stack. A similar operation is performed on the selected X group to perform final read selection.

Current equalizing for the sink and drive groups is performed by four Balun transformer/current-limiting resistor combinations. In the read operation for Y sink bit YS0, for example, the balancing current path is from -12V, through the Y-R secondary (pins 8 and 9) of Balun transformer T28, bit 0 Y sink driver Q20, Balun transformer T6

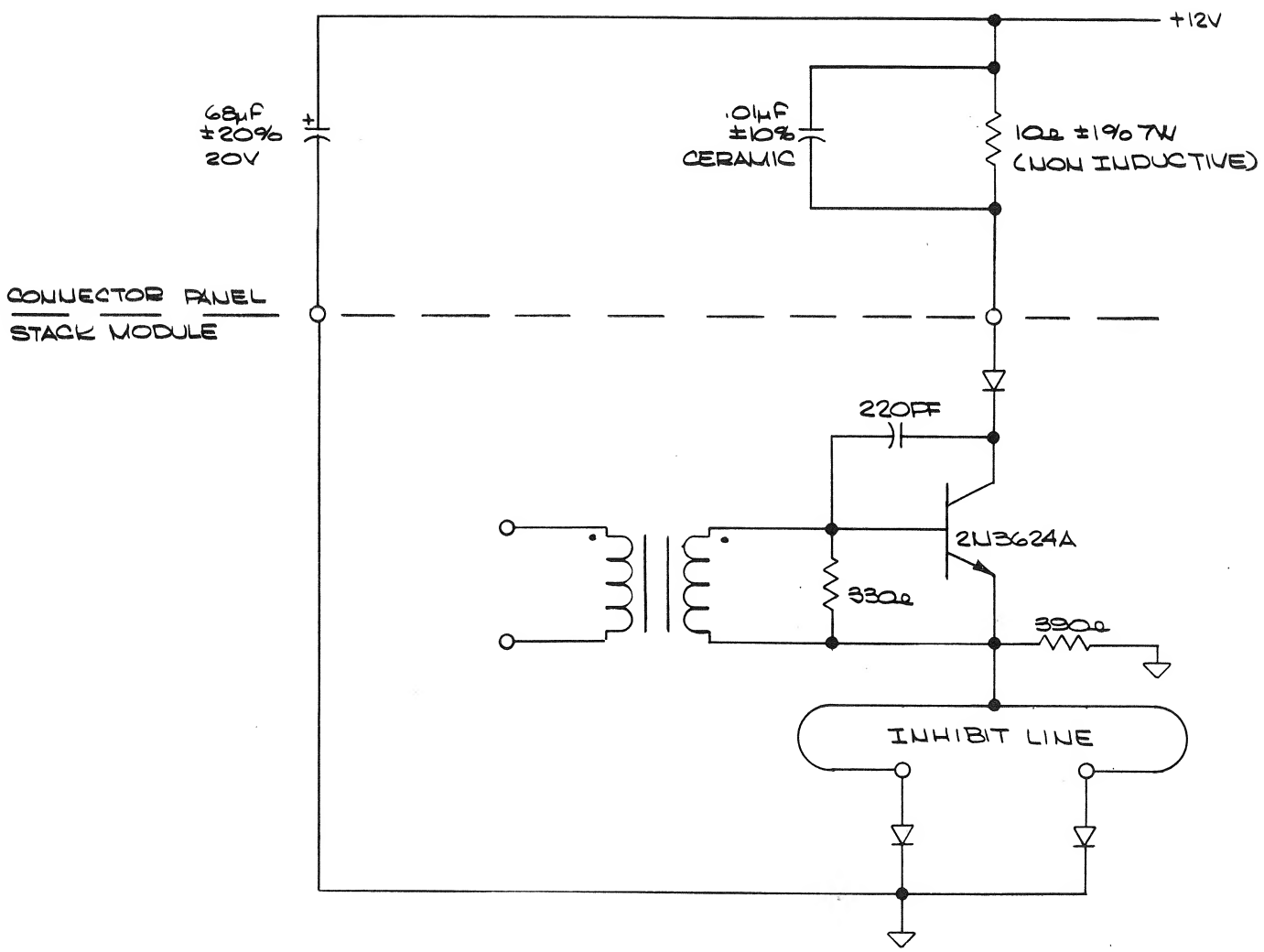


Figure 3-2. Typical Inhibit Current Loop

secondary (pins 15 and 2) the Y drive line in the stack (YS0), Y read bit 0 driver Q45, the Y-R primary of T28, current-limiting resistor R49, to +VDC. In the write operation for bit 0, the balancing current path is similar but opposite in direction through the Y-W section of T28.

3.5 SIGNAL DESCRIPTIONS

3.5.1 Timing and Control

The timing and control board is designed to drive a minimum of one and a maximum of eight 4096 word stack boards of up to 18 bits each. All functions derived by the timing and control board may alternatively be provided by the user if care is taken with the polarity, loading and timing of the respective interface signals.

The following is a list of interface signals for each 4096 word stack module:

3.5.1.1 INTERFACE SIGNALS

Read Timing

Address (12 lines for 4096 words)

Inhibit Timing

Sense Amplifier Strobe

Data Input (Inhibit-Drive, one for each bit of the data word)

Write Timing

Stack Select

Inhibit Current (one for each bit of the data word)

3.5.1.2 RESTRICTIONS

The following paragraphs describe each of the above signals, giving the specific requirements for each in order to ensure reliable operation in the clear/write or read/restore modes at a 1.2 microsecond cycle time. Any deviation from these requirements may cause loss of performance, destruction of components or both.

3.5.1.3 ADDRESS

A total of 12 binary address inputs are needed to decode 4096 words. Each line has a "fan-in" of one unit load to a TTL device for each stack board used. All 12 address lines must be stable at the beginning of a memory cycle (70 nanoseconds prior to the READ TIMING pulse). They must remain stable for 100 nanoseconds after the completion of the WRITE TIMING pulse.

3.5.1.4 STACK SELECT

This input is used to select the correct stack board when 8192 words or more of total storage is used. Only one stack board may be selected during any one memory cycle. To select the required 4096-word stack the respective stack SELECT line should be true (positive) for the same duration and time as the address inputs. If only one stack board is used, this input may be left open or biased to a true logic level.

3.5.1.5 READ TIMING

READ TIMING is a positive-going logic level pulse with a fan-in of one for each 4096-word board. The pulse is used to generate the X-Y read current pulses. It starts the memory cycle and is needed for all memory modes. It should not be earlier than 70 nanoseconds after the latest address and stack select inputs have settled. The pulse width should not be less than 200 nanoseconds or more than 230 nanoseconds.

3.5.1.6 SENSE AMPLIFIER STROBE

This is a positive-going logic level pulse with a fan-in of one for each 4096-word board. It is used to strobe the sense amplifier signal. The pulse width should be a minimum of 60 nanoseconds and a maximum of 80 nanoseconds.

In order to ensure the system margins are at a maximum, the leading edge timing of this pulse is critical and should be adjusted in the following manner:

1. Set the leading edge to approximately 180 nanoseconds later than the leading edge of READ TIMING.
2. Write all ones in the memory.
3. Display on a Tektronix 547 Oscilloscope or equivalent the differential signal at pins 2 and 3 or 6 and 7 of any one of the sense amplifiers.
4. Run the memory.
5. Display the SENSE AMPLIFIER STROBE on the oscilloscope from pin 11 or 14 or the sense amplifier.
6. Adjust the timing to the SENSE AMPLIFIER STROBE such that the leading edge is coincident in time with the peak of the ONE signal at the sense amplifier input.

3.5.1.7 DATA INPUT

One DATA INPUT logic level signal with fan-in of one for each 4096-word board is needed for each bit of the data word. Each line should be stable at least 100 nanoseconds prior to the INHIBIT TIMING pulse to ensure that correct data is written into the word. It must remain stable until at least 100 nanoseconds after the completion of the INHIBIT TIMING pulse. A logic true level on the DATA INPUT time stores a ZERO signal in the core stack; this results in a continuous true level output from the SENSE AMPLIFIER OUTPUT line of that bit.

3.5.1.8 SENSE AMPLIFIER OUTPUT

A ONE must be stored in the core stack to obtain a negative-going logic level SENSE AMPLIFIER OUTPUT. Under these conditions, this pulse appears approximately 100 nanoseconds after the SENSE AMPLIFIER STROBE leading edge.

3.5.1.9 INHIBIT TIMING

This is a negative-going logic level input with fan-in of one for each 4096-word board. It determines the inhibit current time period. Its leading edge must occur no earlier than 350 nanoseconds after the leading edge of READ TIMING. The pulse width must not be less than 580 nanoseconds nor more than 620 nanoseconds.

3.5.1.10 WRITE TIMING

This is a positive-going logic level input with fan-in of one for each 4096-word board. It determines the X-Y write current time period. Its leading edge must occur no earlier than 300 nanoseconds or later than 330 nanoseconds after the leading edge of INHIBIT TIMING. The WRITE TIMING pulse width must not be less than 200 nanoseconds wide, in addition, the pulse must not finish less than 100 nanoseconds before the completion of INHIBIT TIMING.

4.0 MAINTENANCE OF MEMORY SYSTEM

4.1 GENERAL

This section presents information required to maintain the memory system. Included are preventive maintenance, general servicing instructions, troubleshooting, and a replaceable parts list.

4.2 MAINTENANCE PHILOSOPHY

The memory system is constructed on a modular basis. Further, the circuitry on both boards

of the basic system (timing and control board and stack board) are grouped in terms of their functions. This scheme permits a simplified approach to troubleshooting, and isolation and repair of system failures.

CAUTION

The memory system is factory warranteed. Except for standard measurements and checks, detailed servicing by the user may violate warranty. If the system is still within warranty, it is recommended that repair be restricted to replacement of a malfunctioning board assembly. Contact Digital Computer Controls for warranty and service advice before attempting further maintenance procedures.

4.3 TEST EQUIPMENT

Only two instruments are required for maintenance of the memory system other than those normally available in an electronics laboratory. These are as follows:

Digital Computer Controls Memory Exerciser, Part No. 41001351. This instrument is used to stimulate the memory on a programmed basis during detailed tests.

Tektronix Type P6016 Current Probe. This instrument is used to monitor inhibit and drive current at the board current loops in conjunction with an oscilloscope.

4.4 SERVICING

For most memory checkout procedures, measurement of voltage signals at the test points provided on the two boards is all that is required to localize faulty circuits. A list of the signals available at the timing and control board and stock board test points is given in Table 3-2.

Two current loops are provided on the timing and control board for monitoring inhibit current. Four current loops are provided on the stack board for monitoring X-Y read/write drive currents.

4.5 ADJUSTMENTS

All component values are factory selected, so there are no provisions for field adjustment. If system performance is degraded through out-of-tolerance conditions, contact Digital Computer Controls.

4.6 CHECKOUT

Routine memory checkout is best accomplished in marginal power input state with Digital Computer Controls Memory Exerciser. This instrument enables maintenance personnel to stimulate all functional areas of the memory on a systematic basis so that no area of the memory is ignored. The tests described in the following paragraphs should be run with input power in both the +5 percent and -5 percent condition. Memory errors noted can then be subjected to the troubleshooting routines described in paragraph 4.7.

Table 3-2. Test Point Chart

TP	Signal
Timing & Control Board	
1	OV
2	+5
3	Input Data Strobe Z1
4	Input Data Strobe Z0
5	Write Timing
6	Read Timing
7	Sense Strobe
8	Data Bit 9 Output
9	Stack Select 4K
10	Stack Select 8K
11	Stack Select 12K
12	Stack Select 16K
13	Stack Select 20K
14	Stack Select 24K
15	Stack Select 28K
16	Stack Select 32K
17	Data Bit 0 Output
18	*12 Volts
Stack Board	
1	VDC (Drive Voltage)
2	-12V

These checkout procedures first write and read the worst-case data pattern, then execute the same functions with all ZERO bits and all ONE bits. To perform the procedures, proceed as follows:

a) Write the worst pattern (WP=A0+A11) into all memory locations.

b) Sequentially read through all addresses and verify that worst pattern data is stored, error-free, in all locations.

c) Repeat steps (a) and (b) using all ZERO bits instead of the worst pattern.

d) Repeat steps (a) and (b) using all ONE bits instead of the worst pattern.

4.7 TROUBLESHOOTING

Memory system errors fall into three basic categories: timing and logic, address-oriented, and

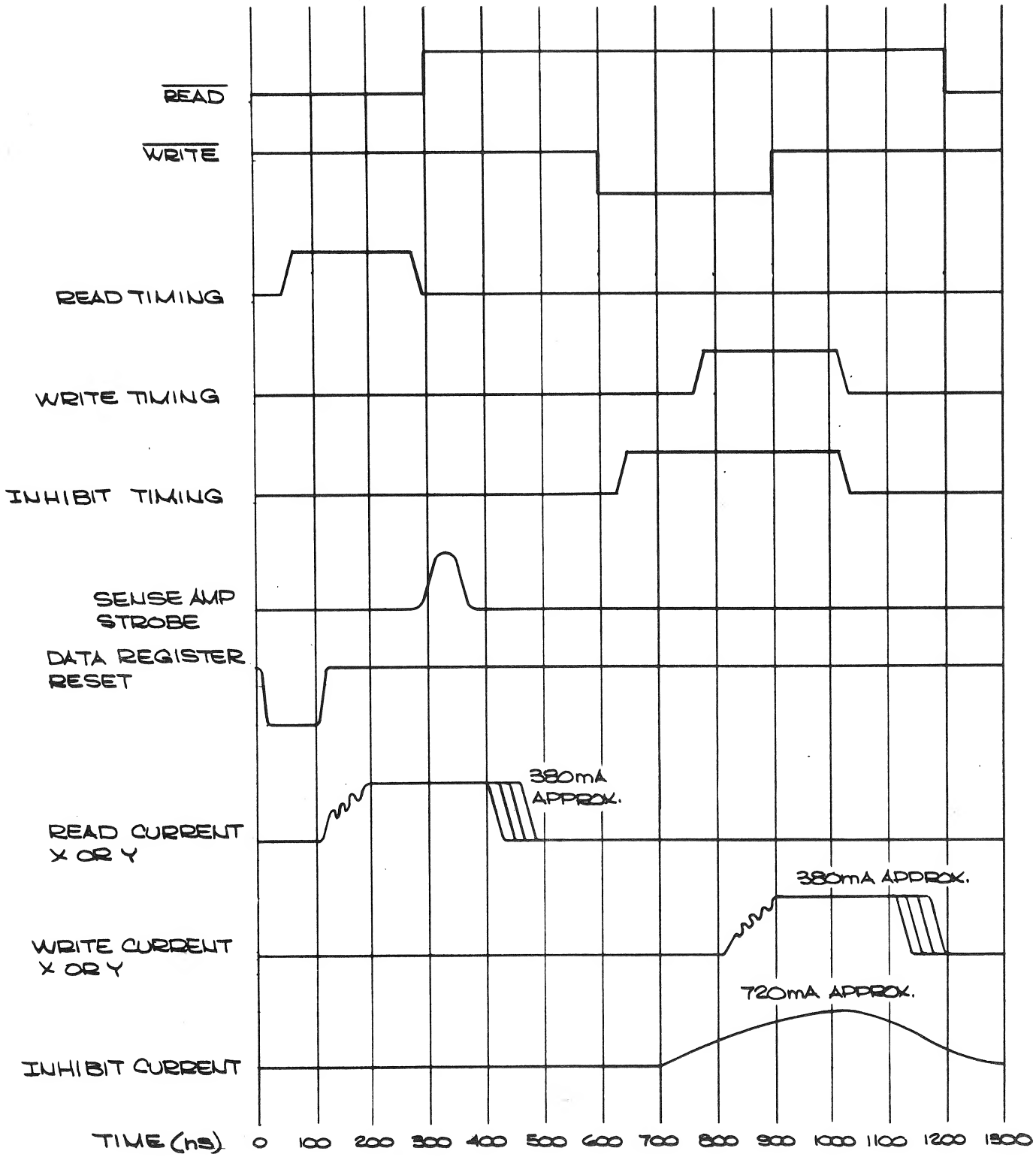


Figure 3-3. Idealized Drive Current Waveforms

bit-oriented. The errors in these three categories exhibit characteristics that are unique to the categories. Through analysis of the error characteristics, the fault can be grossly isolated to either a board or group of circuits on a board. Troubleshooting should proceed on a systematic basis, using the Digital Computer Controls Memory Exerciser to stimulate the memory in a continuously narrowing field (mode and command, stack, address, bit location) until the error is located. Use of the timing diagram and text in Sections 2.0 and 3.0 will facilitate troubleshooting.

CAUTION

Do not attempt to disassemble or repair the core stack. Replace a faulty core stack with a spare and return the faulty core stack to Digital Computer Controls.

4.7.1 Timing and Logic Errors

These errors are characterized by such problems as inability to access the memory, grossly incorrect data transfer, or inability to transfer any data through memory. This type of error can be isolated by observing the timing and control signals at the test points on the timing and control board (refer to Table 3-2). Immediate verification that the problem exists on the timing and control board should be made by substituting a spare timing and control board.

4.7.1.1 No Access to Memory: Failure of the memory system to accept requests for access can be identified by monitoring the test points listed in Table 3-2.

4.7.1.2 Gross Data Errors: If the memory system is accepting READ commands but all data is in error, check the READ TIMING, WRITE TIMING, and INHIBIT TIMING signals. Absence or incorrect timing of any of these signals could cause gross data errors. (See Table 3-2.)

4.7.2 Address-Oriented Errors

These errors are characterized by bad data in some word addresses but good data in the remaining word addresses. The errors are caused by failure of some but not all drive currents. The drive currents can be monitored at the four drive current loops on the stack board.

Figure 3-3 shows the idealized current wave forms that can be monitored through the current loops. The drive current waveforms vary with temperature but, at 25°C, the waveform should represent 380 ma, ± 5 percent.

If a read current but not write current (or vice versa), or X drive current but not Y drive current (or vice versa), is present, the fault is probably on the stack board. Set the Memory Exerciser to stimulate the bad addresses and troubleshoot the X-Y read/write drive line matrix. If only a single address is faulty, suspect a bad decode diode or open drive line for that address. If a group of eight addresses are faulty, troubleshoot the drive switch and circuits associated with the group.

4.7.3 Bit-Oriented Failures

This type of error is characterized by data at all addresses being good except one (the same) bit position in each word. First check the inhibit drive current for the involved bit position, using the inhibit current loop. If the involved bit position is not provided with a current loop, check the voltage at the collectors of the inhibit drivers (Q85 through Q99). If the inhibit drivers are being switched properly, remove stack board power and check the continuity of the involved inhibit line.

SECTION IV

I/O UNIT

1.0 GENERAL

The I/O unit is a printed circuit board Module which enables the computer to communicate with peripheral devices. The I/O PC board is divided into three main sections (see Figure 4-1). They are the External I/O, the Internal I/O, and the console teletype interface.

2.0 DETAILED DESCRIPTION

2.1 EXTERNAL I/O BUS

This section consists of line drivers and line receiver circuits to provide signal coupling with the external equipment through 6 connectors in the D-112 Main-frame. A driver or receiver for each signal lead is provided. The D-112 is normally supplied with a positive logic I/O. The Logic levels are 0 volts (grd) and +3 volts. (Note: A negative Logic External I/O bus can be supplied as an option.)

The I/O supplies both level and pulse signals. They are handled by two different types of drivers, the pulse driver provides an active pull up signal for the output drivers in order to reduce the rise time of the pulse signals. Figure 4-2 shows the level and pulse driver for the positive I/O and the driver for the negative I/O (the negative driver is the same for level and pulse signals).

A detailed description of the I/O and Data Break signals and their respective I/O connector pin numbers is given in Section VI, Installation.

The receiver circuitry of the I/O board provides input diode clamping, and resistor pull up for collector ORing of the peripheral device drivers. Figure 4-3 shows a typical receiver circuit for the I/O positive and I/O negative.

2.1.1 I/O Interconnection Cables

The interconnection cables from the processor to the peripheral device consist of 18 conductor coaxial cables, or flexprint cables terminated in a connector printed circuit board. These cables are connected into the I/O connector panel in the back of the processor, and they are designed to minimize and protect the system against cross talk and radiated noise from the outside world. Section VI, Installation, should be consulted for a detailed description of the device cable interconnection options.

The coaxial cable used for the external options have the following electrical specifications:

Z = 95 Ohm ± 5%

R = .095 Ohms per foot (nominal)

L = 124 μH/ft (approx)

C = 13.75 pf/ft (approx)

Y = 79% of velocity of light, (approx) (approx. 1.5 n/s /ft)

Maximum length of the I/O cable should be 50 feet. These 50 feet of cable can be a combination of coax and flexprint, in which case the total length of the first flexprint should not exceed 15 feet.

Figure 4-4 shows a typical I/O bus configuration for interconnection several I/O devices with the D-112 minicomputer.

2.2 INTERNAL I/O BUS

The Internal I/O Bus uses the I/O control signals, the accumulator and memory buffer signals directly from the processor, which are available at the input pins of the I/O board. The input data signals into the I/O system are ORed into a two input nand gate with the external I/O bus. This signal is called INTI/O, and they are pulled up to +5V by a resistor in order to provide collector OR capability for different devices.

2.3 CONSOLE TTY

The I/O interface board (positive or negative) provides the control logic circuit for interfacing the processor with a local teletype. The teletype interface is divided into two main sections, corresponding to the transmit and receive operation of the teletype. Both sections use a common uni-junction clock circuitry for their timing operation. This uni-junction time circuitry is an ultra-stable RC oscillator circuit. The precision of the circuitry is 1% under extreme temperature variations, and its frequency can be adjusted by a potentiometer supplied directly at the top of the board. Two test points are also supplied for this operation. One of these test points corresponds to the clock output, and the other test point corresponds to the ground of the system. Normal adjustment of this clock period is 1.1 milliseconds for the regular ASCII teletype code.

A power clear signal is provided to reinitiate the I/O bus interface when the power is turned on or when the START key or RESET key is depressed on the front panel of the processor.

The I/O interface PC board provides standard TTY signals from the logic level signals of the processor for directly controlling the teletypewriter, including an AC relay to provide control of the teletype tape reader from logic level signals. This circuit is mounted at the teletype itself, and transfers

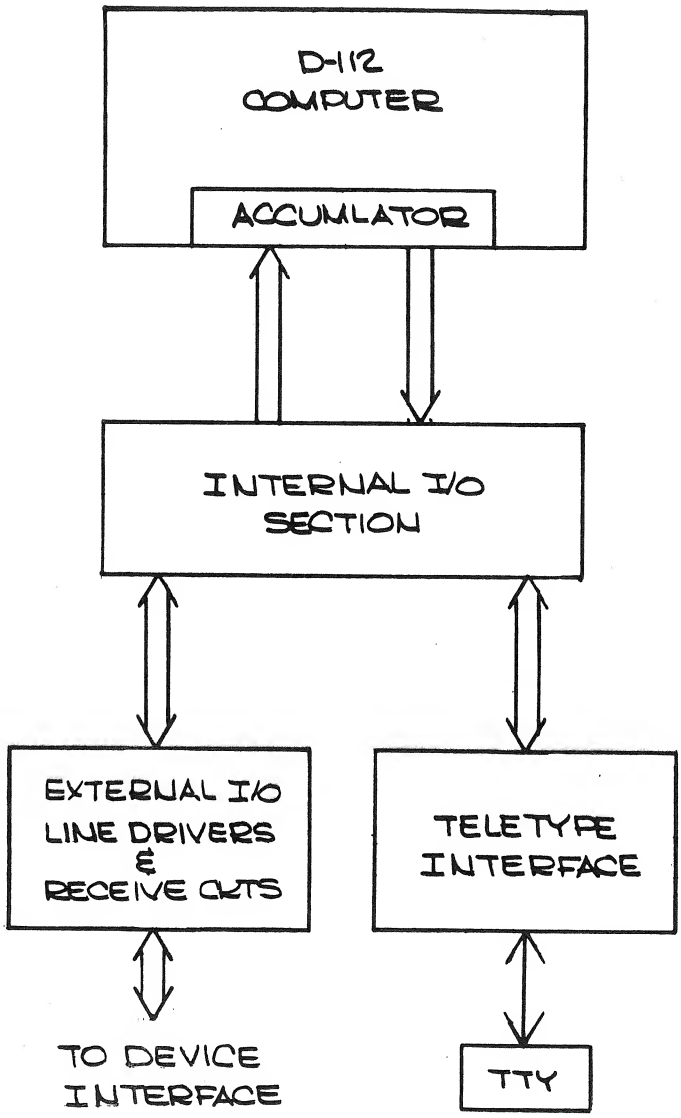


Figure 4-1. Block Diagram of I/O Unit

command from the DC logic levels to the AC power levels required by the teletype tape reader. (See circuit diagrams in Volume II of this Installation & Maintenance Manual.)

2.3.1 Transmit Section

The teletype interface allows the processor to transfer the 8 bits of parallel information stored in the accumulator into a disassembly register which converts this information to a serial train of pulses for direct transfer into the teletype. Also provided in this section is control over the stop bit length for different applications, and flag control to inform the processor when the transfer of information has been completed.

The operation of this transmit interface is completely controlled by the processor with the use of three different IOT instructions. These IOT's are decoded with the IOP and they provide all the logic control functions for the operation of this interface.

A detailed description of the operation of I/O instructions is given in Section II, paragraph 4. Figure 4-5, Transmit Timing Diagram, and the I/O Logic diagrams should be consulted as reference during this section.

2.3.1.1 Load Teleprinter and Print (TPC)

The instruction 6044 (Octal) transfers the contents of accumulator bit 04 to 11 into the disassembly register of the interface. The teletype I/O decode combined with INTIOP4 pulse enables the LTBFF signal that enables the input of the direct set control input of the disassembly register, transferring the contents of the accumulator bit 04 to 11 into the disassembly register bit 1 to 8. At the same time this information is being transfered into the disassembly register, the START CLOCK flip-flop is set in order to initiate the serial transfer of information. This flip-flop sets to a one the D input of the CLK enable flip-flop. This flip-flop is freely clocked by the XMITCOK timing pulse from the main clock generator. This flip-flop is set at the next

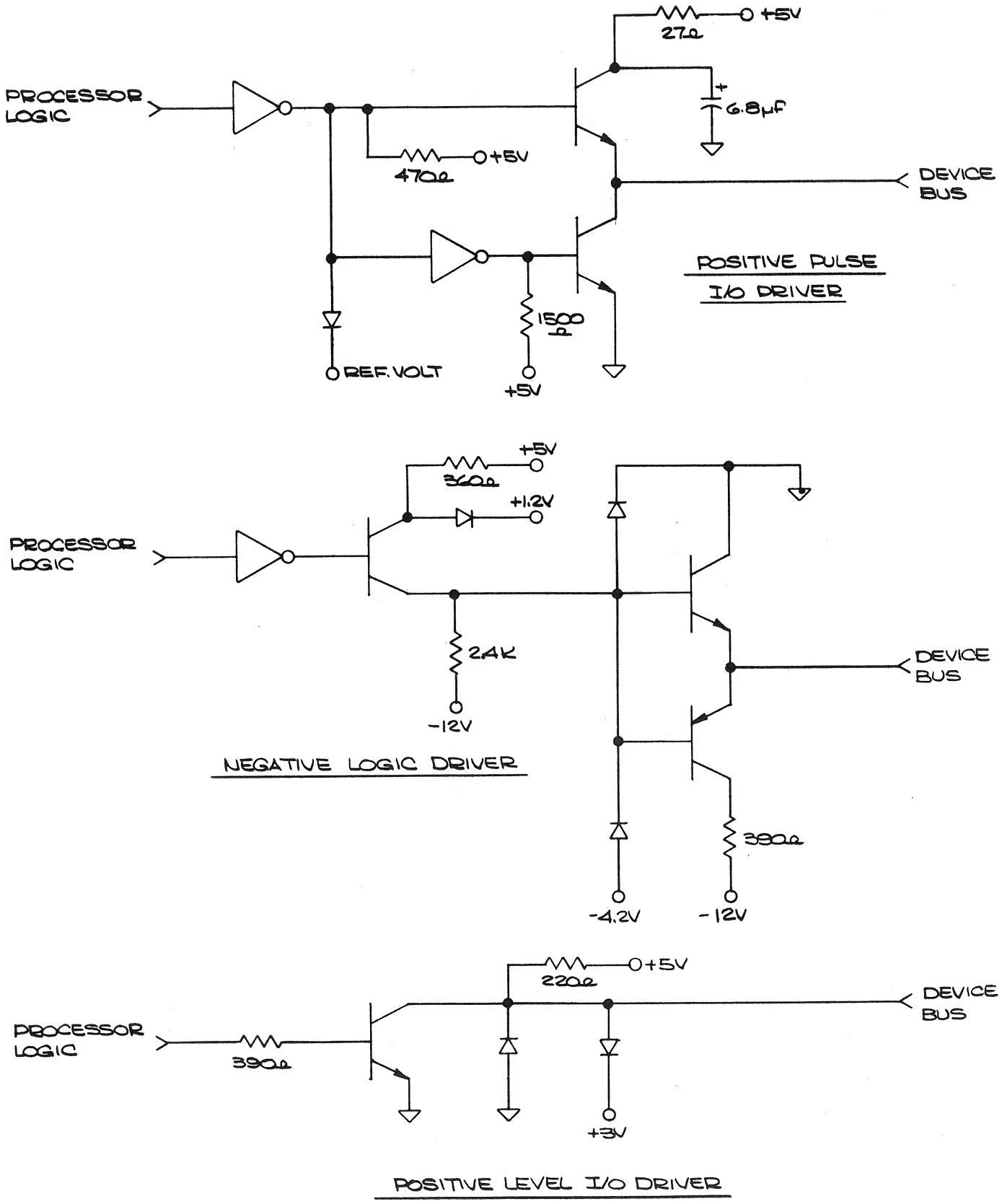


Figure 4-2. I/O Logic Driver

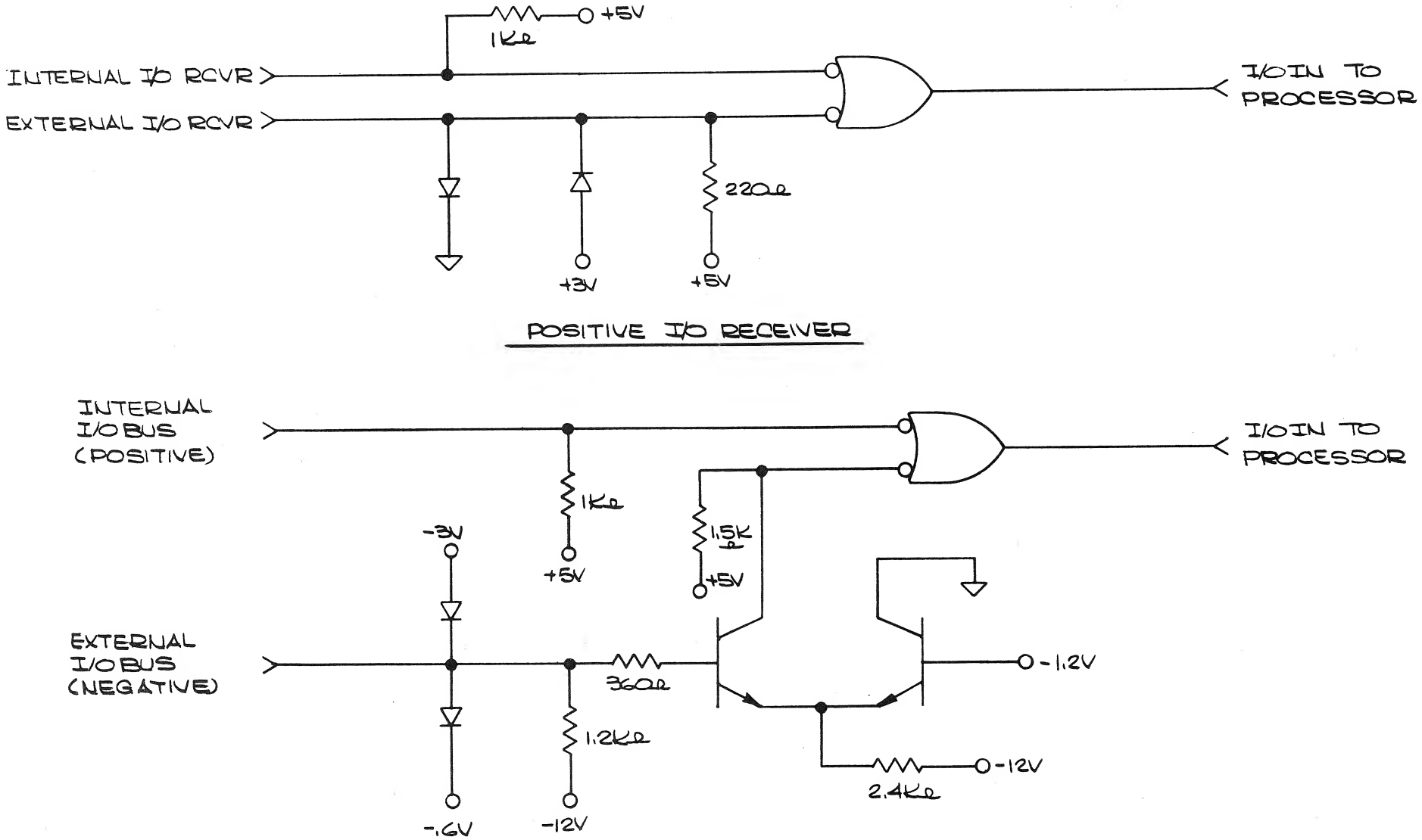


Figure 4-3. I/O Logic Receiver

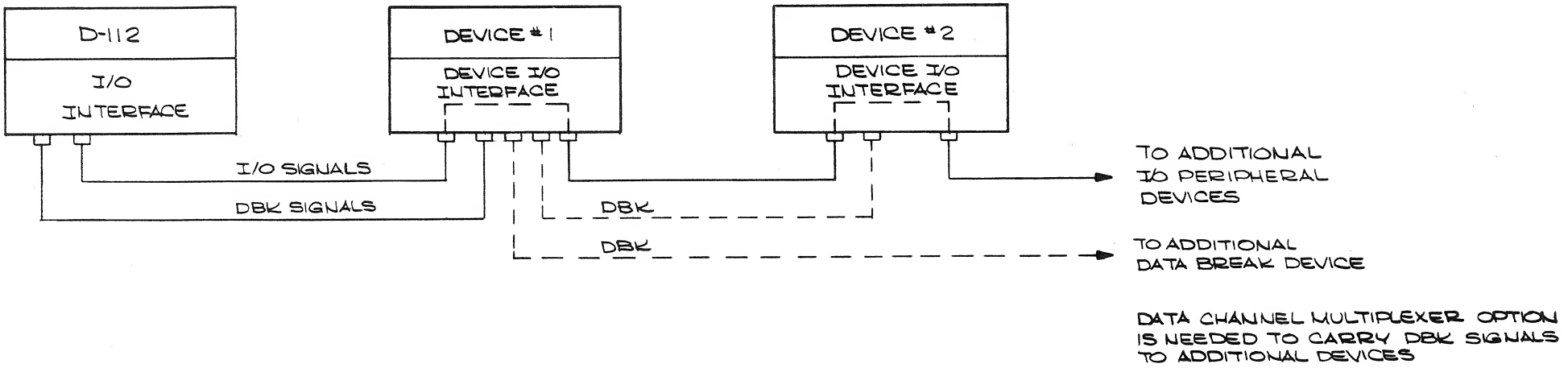


Figure 4-4. D-112 I/O Bus Interconnection

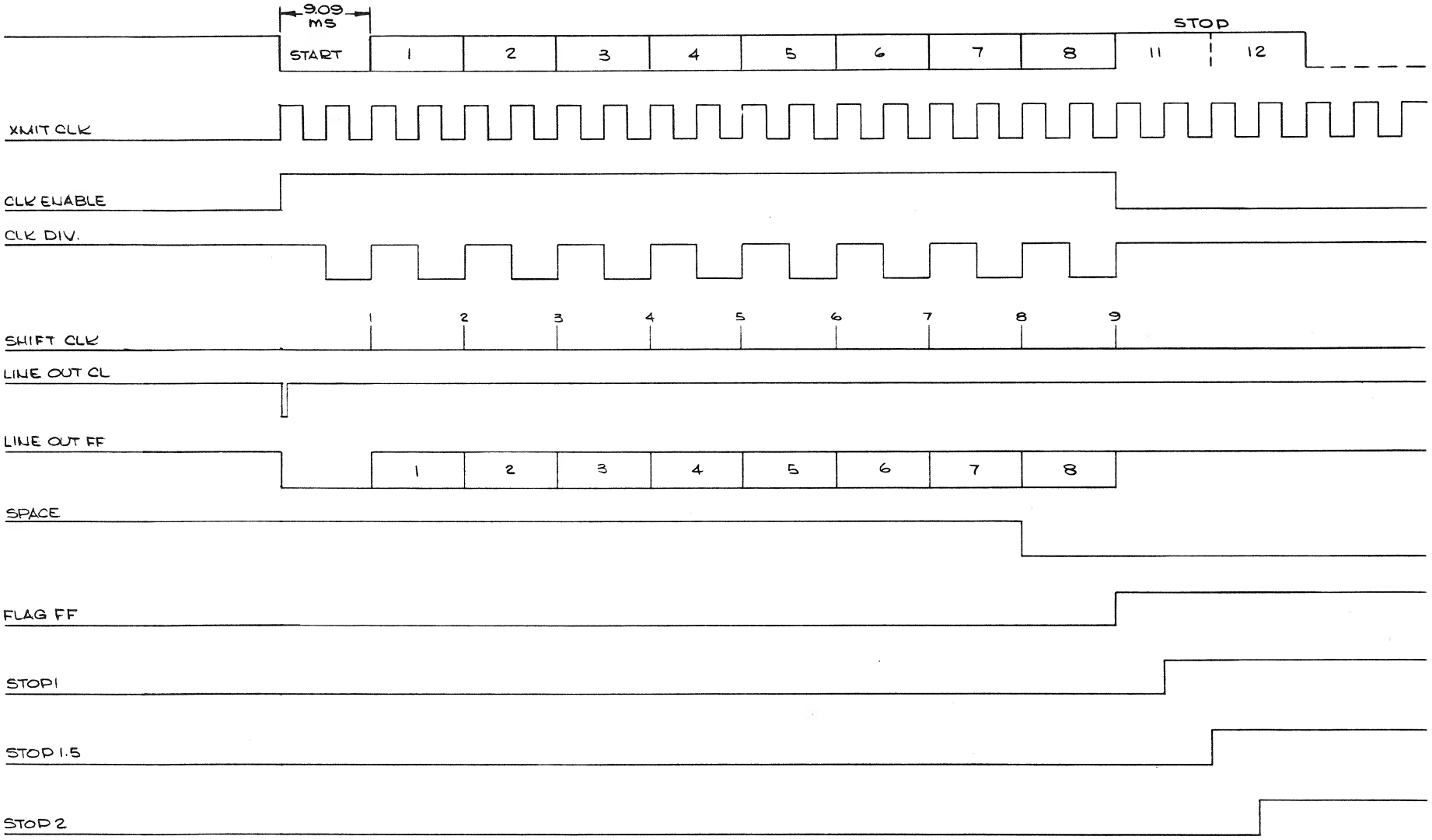


Figure 4-5. Teletype Transmitter Timing

timing clock after its input is set to a one. When the CLK enable is set to 1, it sets to one the preset input of the LINEOUT flip-flop which controls the transmission line to the teletype. It also issues, through a different circuit, a clear signal to this LINEOUT flip-flop setting it to low, producing the start bit into the TYLINEOUT input to the teleprinter. By this means the load assertion START pulse of the character to be transmitted to the teletype is produced after the issue of the IOT command.

The CLK enable flip-flop also enables the D input of the CLOCKDIV flip-flop which divides the frequency of the transmit clock in half, in order to produce the shifting clock signal into the disassembly register. This SHIFTCLK signal is produced every 9.09 milliseconds for regular teletype ASCII code. Nine consecutive shift clocks are issued by the clock divide flip-flop, in order to shift the data stored at the disassembly register one bit at a time into the LINEOUT flop. Every time that a shift command is issued the higher order bit is shifted into the lower order bits of the disassembly register, and bit 1 is shifted into the line out flip-flop. The START CLOCK flip-flop is being activated also by the shift clock, but it's set and reset inputs are such that zero is being shifted from it into the higher order bits of the disassembly register. After eight bits the disassembly register between bits 2 and 8 and START CLOCK flip-flop, contains all zeros, which causes the SPACE Logic signal to be generated. This SPACE signal informs the control in the transmit section that a full character is to be completely disassembled at the next shift clock pulse. The SPACE signal also enables the input of the FLAG flip-flop, which is set at shift pulse No. 9 in order to inform the processor of the completion of character transmission. The SPACE signal also resets the CLK enable flip-flop which resets the CLOCKDIV flip-flop and stops the shift clock into the register. The CLK enable flip-flop also sets the LINEOUT flip-flop into a logical one in order to force the MARK (high) state onto this line. The CLK ENABLE flip-flop also enables the stop counter register. The stop counter register provides the selection of the length of the stop bit of the character being transmitted. There are typically three stop bits to be selected. Stop one which corresponds to one bit stop length, stop 1.5 and finally stop 2 that corresponds to a stop of 2 bit lengths (19.19 milliseconds). The length of the stop bit in the character being transmitted can be selected by using the appropriate jumper provided in the I/O interface board. It should be noted that the interface tells the processor regularly through the FLAG flip-flop of the completion of the signal transmission, and it does not allow the processor to transmit a new character until the stop counter reaches the selected jumper in the I/O board. It should also be observed that the teletype transmitter interface generates the start and stop signals of the teletype signal; the processor only supplies the information bits.

External WAITCONT and BUSY signals are provided for other options of the teletype interface.

A jumper is provided for the selection of the START SELECT signal in order to adapt the interface to a system of 5 or 8 bit character codes.

2.3.1.2 Clear Teleprinter Flag (TCF)

This instruction 6042 (Octal) clears the FLAG flip-flop of the teletype transmitter interface.

2.3.1.3 Skip on Teleprinter Flag (TSF)

This instruction 6041 (Octal) enables the FLAG flip-flop into the internal skip line of the I/O board (XMYT SKIP). For a detailed description of the use of the last three teletype transmitter IOT instructions, the D-112 User's Handbook should be consulted.

2.3.2 Receive Section

This interface circuitry provides the means for the assembly and buffering of the serial information from the teletype to be transmitted into the computer. The interface provides an assembly register, a receive flag register (which informs the processor when a full character has been completely assembled), clock control circuit, stop bit selection, and a teletype reader control circuit. Refer to Figure 4-6 (Teletype Receiver Timing), and the I/O Logic diagrams (Vol. II - Installation and Maintenance Manual) for further details.

The operation of the teletype receiver is initiated under control of the teletype input line. The TLINEIN transmits the serial information from the teletype to the processor. Normally, it is "high" when no character is being transmitted by the teletype. When a character is transmitted, the first bit is always "Low", which enables the signal LINEIN. This signal provides a double control function on the receiver circuit. First, it enables the clock divider register, a three bit ripple counter for division of the receiver RECVCLK timing clock. The second function of the LINEIN is to enable a clear signal ANDed with the CLKDIV1, in order to clear the assembly register before the assembly of the teletype character. This clear signal also resets the READER CONTROL flip-flop, and the STOP register (bit 1 and bit 2). The READER CONTROL flip-flop disables the teletype reader circuit in order to enable the reader to step to the next character of the tape during the time that one character is being assembled by the assembly register.

The CLKDIV 3 flip-flop sets the START CONTROL flip-flop which enables and controls the operation of the clock divider ripple counter. This operation provides a half bit noise spike detector in the teletype receiver. This is accomplished by the direct clear of the teletype input line over the clock divider ripple counter circuitry, if a spike to ground that is less than half of the bit length of a start bit is detected by this circuit. The LINEIN signal clears the clock divider ripple counter inhibiting the START CONTROL flip-flop from being set.

The start control flip-flop allows the clock divider counter to enable the SHFCK assembly clock for shifting the information of the teletype LINEIN input into the first bit of the assembly register. The shift clock of the assembly register is issued within the period of the start bit, and any data bits of the teletype signal. This will provide time for sensing the data coming from the line, avoiding false data assembly, from distorted signals. After nine consecutive shifts through the assembly register, the start bit will be stored at the RECFLAG flip-flop. This will inform the processor (over the interrupt and skip line) that a full character has been assembled. The STOP control flip-flop is set at the same time as the FLAG flip-flop. This STOP control flip-flop inhibits any further shift clock signals to the assembly register, and inhibits the clear signal of the assembly registers. It also keeps the clock divider working to provide the counting of the STOP pulse. The STOP counter will count the 1 or 2 stop bits (depending upon the selection of the stop bit jumper located on the I/O board) and then will clear the stop control flip-flop in order to allow the assembly register to receive the next character. When the STOP control flip-flop is reset, it will clear the clock divider ripple counter in order to re-synchronize the timing of the receiver interface with the new start bit of the next character to be assembled. It should be observed that the information assembled in the assembly register remains up to the leading edge of the START bit of the following character at which time a CLEAR signal is generated. NOTE that the stop signal of the received character is received in the interface, but is not transmitted to the processor.

Three IOP instructions are used to communicate with the computer.

2.3.2.1 Skip On Keyboard Flag (KSF)

This instruction 6031 (Octal) enables the output of the REC FLAG flip-flop onto the internal I/O skip line (REC skip).

2.3.2.2 Clear Keyboard Flag (KCC)

This instruction 6032 (Octal) clears the RECFLAG flip-flop when the character has been transferred from the assembly register into the accumulator of the computer. This instruction also sets the READER CONTROL flip-flop to enable the TYREADERCONT signal, enabling the teletype tape reader to read the next character.

This IOT instruction also enables the INTACC-CLEAR signal inhibiting the enable input signal of the accumulator into the input multiplexer during an IOT instruction and clears the accumulator.

2.3.2.3 Read Keyboard Static (KRS)

This instruction 6034 (Octal) enables the output of the assembly register into the internal I/O bus of the processor. The assembly register bits 8 to 1 are enabled into the internal I/O bits 4 to 11 respectively.

NOTE: A series of jumpers are provided on the I/O board to allow the assembly register to receive 5-bit or 8-bit character codes.

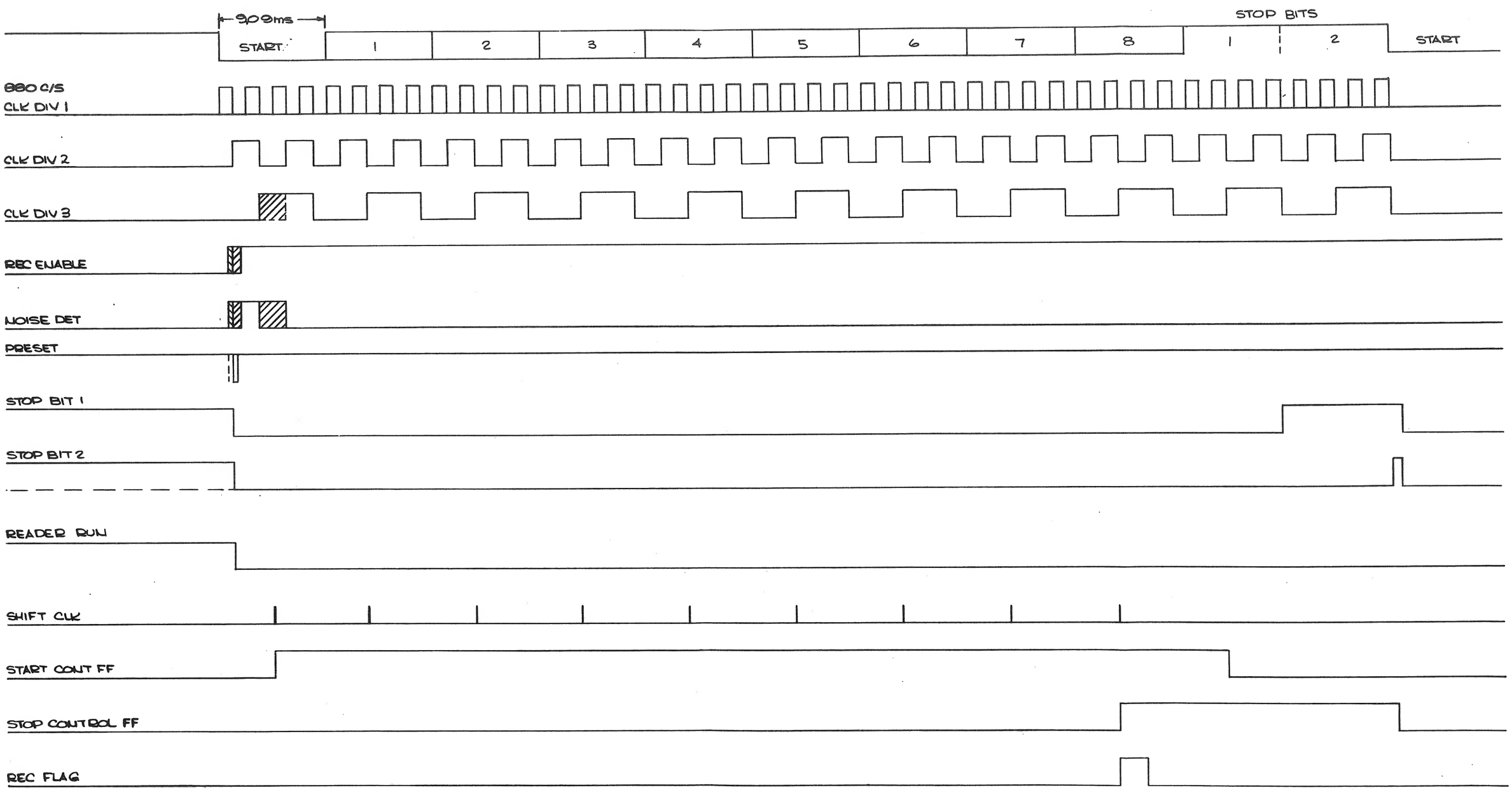


Figure 4-6. Teletype Receiver Timing

SECTION V

POWER SUPPLY

1.0 GENERAL

The power supply consists of three transistorized series regulated (+12V, +5V and -12V) outputs and one unregulated output (+17V). It is cooled via an adjacent exhaust fan located in the computer which draws air through the computer, then the power supply. The power supply will not operate properly without forced air cooling.

2.0 DESCRIPTION

2.1 INPUT

The input power range is 115VAC ±10% 50/60HZ, single phase 4 Amps. All of the outputs pass through a PCB edge connector located at the top of the power supply. The AC power enters on the rear panel and is relay controlled by a front panel key switch on the computer.

2.2 THERMOSTATIC CONTROL

The ±12V supplies are sequenced on and off in conjunction with a "Power on" signal generated within the power supply. An internal thermostat which breaks the AC line is set to trip when a fan failure or ambient over-temperature condition exists. The thermostat trip causes the unit to turn OFF for 5 to 10 minutes (until the internal temperature drops) and automatically returns to ON. The power supply sustains DC output power during any 5 MS or less AC line "down" transient. Any transient longer than 5 MS causes the power supply to sequence OFF and then sequence ON approximately 100 MS after re-energization of the AC line. In order to lengthen the transient immunity from 5 MS to 50 MS, an additional energy storage bank must be used (external from the computer) which plugs in a second PC card edge connector located on the inside of the power supply in the same plane as the output connector.

2.3 ACCESSORY OUTLET

A dual AC accessory output (with equipment ground) is switched on and off by an internal relay. The load capability is 11 amperes maximum.

2.4 RADIO FREQUENCY INTERFERENCE (RFI)

High radio interference noise producing equipment such as electric drills, heat guns, etc., should not be used in the accessory output, as they may cause improper operation during normal running of the computer.

2.5 CONTROL CIRCUITRY AND FUSING

The PC card located in the top of the power supply contains all of the control circuitry and can be removed without removing the power supply from the computer. A single mounting screw located near the rear panel, holds it in place. All of these boards are electrically interchangeable and may be used in any power supply.

In addition to the fuses located on the rear panel, there are internal fuses which are used for protecting the unregulated +17V and the catastrophic over-voltage failure mode for the three unregulated outputs. Only the +17V fuse (4A clip mounted) can be changed without removing the power supply from the computer. If any of the over-voltage protection fuses blow, the power supply must be removed in any event, to correct the failure.

2.6 ADJUSTMENTS

The three regulated outputs can be voltage trimmed or changed during marginal testing from the top of the power supply. Only the top cover of the computer must be removed to get to the three pots located on the plug in PC card. Each pot is marked as to which output it controls. The ±12V supplies track each other when adjusting the +12V pot, and the -12V pot is used to align its voltage with the +12.

3.0 SPECIFICATIONS

Table 5-1 contains power supply specifications.

Table 5-1. Specifications

Voltage	Current Maximum*	Ripple Maximum
+17VDC	Zero to 4 Amps	2VPP
+12VDC	Zero to 6 Amps	25MVPP
+ 5VDC	Zero to 15 Amps	25MVPP
-12VDC	Zero to 3 Amps	25MVPP
Start Signal + 4VDC	10MA	25MV
3VAC Line Frequency	10MA	
115VAC Fan Power Line Frequency	175MA	

*These currents are maximums and not necessarily the currents being drawn by the computer.

4.0 THEORY OF OPERATION

4.1 AC INPUT

The 115VAC input is applied to A2-P1 located on the rear panel, and is then passed through A2-F1, A2-K1A, A2-F2 and A2-S1 before entering Transformer T1. Fuse A2-F1 protects the AC line from both power supply internal shorts and external shorts on the 115V accessory duplex plug output. Fuse A2-F2 protects for internal shorts in the power supply. Thermostat A2-S1 protects for an over-temperature condition which would exist either through excessive ambient temperatures, fan failure or fan air flow blockage. Thermostat A2-S1 is automatically reset after a thermal trip and automatically closes when reaching a predetermined lower temperature. Relay A2-K1 applies the AC voltage to the transformer of the power supply. A2-K1 coil is energized through the front panel key switch in the computer. Capacitors A2-C1, A2-C2 and A2-C4 are for high frequency noise suppression generated in the relay and from outside sources. Transformer T1 also supplies voltage to the blower located in the computer chassis.

4.1.1 Line Voltage

The normal AC input voltage range is 105 to 125VAC.

4.2 UNREGULATED SECTION

Transformer T1 consists of a center tapped power winding with two taps and a small center tapped bias winding. The bias winding feeds rectifiers on the A2-A1 plug in P.C. card, which provides +34V and -27V unregulated bias supplies. These supplies are used to run the amplifiers and sequencing circuits and are discussed at a later time. The main power windings are connected directly to the power diodes A2-CR1 through A2-CR6 mounted directly on A2 mother board. These diodes in turn feed three capacitor input filters, the +17V, +9V and -19V. These voltages feed the +17V unregulated, +12V regulated, +5V regulated and the -12V regulated, respectively. Each of the regulated outputs are protected with a clip fuse mounted directly on the printed circuit mother board. A2-F3 protects the +12V supply, A2-F2 protects the +5V supply, and A2-F1 protects the -12V supply. These fuses should only blow from a failure in the series regulators, which in turn would cause the output to be crowbarred or shorted down to ground through an SCR. Therefore any supply with this fuse blown most likely has an internal failure and should be checked before reinstalling in the computer chassis. The +17V unregulated output has its own fuse A2-F4 and can be changed by removing the top cover of the computer. The fuse is located horizontally above the connector of the A2-A1 plug in P.C. card. Each filter capacitor has a small bleeder resistor across it which allows the capacitor to discharge during the time it takes the power supply to be removed from the computer.

4.3 SERIES REGULATORS

The pass transistors for the +12V, +5V and -12V are located on the finned aluminum heat sinks mounted on the back panel (assembly A-1). Each transistor has an associated emitter resistor from which is derived over current protection, signal and transistor balancing. In the case of the +5V supply, these transistors are A1-Q2 and A1-Q3. Transistor A2-Q1 is the transistor for the +12V, A2-Q2 is the transistor for the +5V and A2-Q3 is the transistor for the -12V supply. Capacitor A2-C6 is an oscillation suppression capacitor for the -12V supply. Capacitors A2-C5, A2-C8 and A2-C7 are output capacitors for the +12V, +5V and -12V supplies, respectively. Capacitor A2-C3 is an auxiliary output capacitor located on the back panel of the main assembly for the +5V supply.

4.3.1 SCR Crowbar Circuits

Each regulated supply has its own individual overvoltage protection located on the A2 printed circuit card. Each circuit consists of an SCR and gate to cathode resistor, a firing zener and a firing current limiting resistor. In the case of the +12 supply, these parts would be A2-CR8, A2-R3, A2-CR7, A2-R2, respectively. For the remaining two circuits SCR's A2-CR10 and A2-CR13 are the SCR's that handle the protection. Firing occurs when the output voltage of the supply exceeds the firing zener voltage plus the gate to cathode voltage of the SCR, then current begins to flow into the gate. This fires the SCR into the conducting region and pulls the output voltage down to approximately 1 to 2 volts. If the overvoltage was induced by an outside means, the series regulators go into overload and inherently protect themselves in this partially shorted mode. To unlatch these SCR's the AC line must be removed for at least 5 seconds and then re-energized. The SCR gates to the +12V and -12V supplies also go to the control card A2-A1 which provides a trigger pulse during AC line turn-off. The A2-A1 card provides a control shutdown which is discussed in a later section.

4.4 AC LINE FREQUENCY OUTPUT

A portion of the bias winding from T1 which connects with the A2-A1 plug in P.C. card provides an AC signal through divider A2-R8 and A2-R9. The output line frequency signal is used to clock circuits within the computer.

4.5 A2-A1 PC CARD

This card can be broken down into six basic blocks.

Block #1 - +12V regulator and over-current protection circuit.

Block #2 - +5V regulator and over-current protection circuit.

Block #3 - -12V regulator and over-current protection circuit.

Block #4 - ±12V SCR unlatch circuit.

Block #5 - Sequence circuit

Block #6 - Rectifier circuit for bias supplies.

These circuits show up on the main assembly schematic. For detailed component values, refer to the A2-A1 P.C. schematic.

4.6 +12V VOLTAGE REGULATOR

The +12V regulator consists of a single voltage amplifier driving three emitter followers, two of which are located on the mother board on A1 heat sink assembly. Q10 is the third emitter follower which is located on the control board, and is driven by voltage amplifier Q13. The collector load for Q13 is R21. Q13 receives its base drive from the divided down output voltage via resistive divider R34, R31 and R33. The base voltage or center point on the divider is compared to a stable reference voltage generated in zener diode CR15. CR15 is fired with resistor R25 from the +12V output. If the output voltage goes high, the base of Q13 goes high, and with the emitter remaining fixed, the collector drive point or base of Q10 is pulled down toward common. Thus its emitter is pulled down toward common, thereby pulling the second and first stage emitter followers down, reducing the output voltage. This completes the DC regulation loop.

Transistor Q11 is an over-current protection transistor which is connected into a divider; one end of which looks at the output current with a positive going signal, and the other end looks at the output voltage with a negative going signal. The positive end of the divider is R22; the negative end of the divider is R30. The positive and negative voltage ends as described are with respect to the emitter of Q11. If the output current goes high above a predetermined value, the top of R22 goes positive, turning on Q11, and shunting the drive from Q10 base into the collector of Q11, thereby reducing the output voltage. As the output voltage is reduced, the negative signal on the bottom of R30 is reduced, causing the base of Q11 to be turned on even harder, forcing more base drive from Q10 to be shunted through Q11 as the circuit cascades down to a few amps of idle current at full short circuit. This circuit is commonly known as a foldback type of short circuit protection. R68 provides a little positive foldback which causes slightly sharper characteristics. RC network C9 and R29 consist of a roll off network which controls loop response and DC stability. R28 is a shut off resistor for the base of the second emitter follower located off the printed circuit card.

4.7 +5V SUPPLY

This supply is identical to the +12V supply with the following exceptions: The input voltage amplifier is now differential, consisting of transistors Q15 and Q16. The output voltage is connected directly into Q16 base via limiting resistor R34. The reference voltage is generated in CR16 (5.6V), which in turn is fired from a higher stabilized voltage generated by CR7 (13V). CR7 is fired via R45 and R17 which are connected to the +34V unregulated bias supply. CR7 then feeds CR16 through R59. CR16's voltage is then divided down to 5V through R39 and R40. All other aspects of this circuit, such as the foldback and first emitter follower stability networks, etc., are similar to the +12V supply.

4.8 -12V SUPPLY

This supply is similar to the +12V supply with the following exceptions: The collector source for Q17, is an input voltage amplifier that acts as a constant current generator consisting of Q21, R52 and R73, CR18 and CR19. The reference voltage for this supply is the +12V supply, from which a divider is connected to the -12V supply. The center point is connected to the base of Q17 with the emitter tied to a positive .6V point generated by CR12. This is to establish a zero input at the base of Q17. CR12 is fired with R16 from the +34V bias supply. Over-current protection transistor Q18, emitter follower Q19 and voltage amplifier Q17 all perform in a similar manner to their complementary parts in the +12V supply.

4.9 BIAS SUPPLY

Input AC voltage is applied to resistors R1 and R2 through diode bridge CR1 through CR4 and CR17 to capacitors C1 (positive) and C4 (negative). C1 filters the positive +34V unregulated bias supply powering the on/off sequence circuit, the +12V SCR unlatching circuit, the +12V and the +5V regulators. C4 filters the -27V unregulated bias supply and then supplies a portion of the -12V SCR unlatching circuit, along with the -12V regulator.

4.10 SEQUENCE ON/OFF CIRCUIT

The AC unfiltered ripple through the positive portion of the input bridge is applied to Resistor R3, filtered with C2 and applied to the base of Q1. This circuit is used as an AC line presence detector. When the AC line is present, Q1 is in an ON state, thereby turning off Q2 and Q4. Q4 provides the sequence signal to the computer which is high when Q4 is off. Q2, which is also off, allows the +12V third emitter follower to move freely up to 12V. If Q2 were ON, the third emitter follower Q10 base would be pulled down to near ground, thereby causing the +12V output voltage to be near zero.

Q3 provides a turn on signal to Q4 with a built-in R.C. delay. When the +12V rises during turn on, capacitor C3 begins to charge up. Q3 at some point later gets turned on after the +12V supply is up. After turning on, its collector is low, removing the turn on signal or the base drive from Q4, thereby allowing the sequence signal to come up. Q4 has two base drive sources; one from Q3 collector resistor, and one from Q1 collector resistor. Both Q3 and Q1 must be in the ON state in order that

Q4 be cut off. When Q4 collector goes down during sequencing, Q6 is turned off due to a lack of base drive from Q4 collector resistor. As Q6 goes off, Q5 is turned on, thereby starting a one-shot trigger; the trailing edge causes Q8 to turn off and Q9 to turn on. Q8 is located from gate to cathode of the +12V SCR crowbar. Q9's collector is connected directly to the gate of the -12V crowbar.

The +12V and -12V crowbars fire simultaneously, causing their respective output voltages to fall rapidly within a microsecond or two to 1V. After the firing, transistor Q2 is also in the ON state, and pulls the anode voltage of the +12V SCR below its holding point. This unlatches the +12V SCR and makes it ready for a new turn on sequence. The -12V SCR is unlatched from Q12, being turned on due to the fact that the +5V supply voltage is up and holding. The -12V SCR emitter is attached to the +5V supply, and the +12V supply is down, because its base is attached to it. This in turn causes Q12 to turn on hard, and pulls the -27V regulated through dropping resistor R74 up toward +5V. The -12V supply cuts off, thereby unlatching the -12V SCR. After the ±12V SCRs are unlatched, the power supply is ready for another turn on sequence.

4.10.1 Turn On Sequence

The following circuit functions are in order of turn on sequence.

1. AC line energized - +34V up, +5V up, Q2 on, Q3 off, Q4 on.
2. Q1 turns off, Q2 off, +12V supply up, -12V supply up.
3. Q3 turns on - Q4 off, sequence signal up.

4.10.2 Turn Off Sequence

1. AC line deenergized - Q1 off, Q4 on, sequence signal down.
2. Q8 is cut off, Q9 turned on, ±12V SCRs fire, ±12V supplies go to around 1V.
3. Q2 turns on, +12V SCR unlatches.
4. Q12 turns on, -12V SCR unlatches.
5. Ready for sequence on.

4.10.3 Nominal Sequencing Times

ON

+5V	25MS
±12V	60MS
Sequence Signal	90MS

OFF

Sequence Siganl	6MS
±12V	8MS
+5V	12MS

A down transient or missing portion of the AC input for less than 5MS does not cause the power supply to sequence OFF. Any voltage drop to zero of more than 5MS causes a sequence off cycle. If the AC lines goes off for 10MS and comes back, a delay of 100 to 200MS is automatically provided in the supply before sequencing back ON. An external capacitor can be used to lengthen line transient immunity from 5MS to 25MS and 50MS with optional external energy storage banks, that can plug in to the power supply at the inside rear, near the signal cables. Longer durations can be provided on special request.

5.0 TROUBLE SHOOTING CHART

Table 5-2 provides a Trouble Shooting Chart. The numbers 1 through 4 indicate the first most probable failure to the fourth most probable failure for each of the symtoms.

Table 5-2. Trouble Shooting Chart

PROBABLE FAILURE	SYMPTOMS										
	+5V Low or Near Zero	+12V Low or Near Zero	-12V Low or Near Zero	+17V Low or at Zero Volts	Input Fuses Blow at Turn On	Thermostat Trips When Unit Is Hot	Output Voltages Sequence Improperly	No Voltage from Accessory Output on Rear Panel	Sequence Down Starts Prematurely on AC Line Transients	Power Supply Will Not Turn On	Power Supply Will Not Turn Off
Series Regulator Failure Caused Overvoltage Condition which in turn blow Internal Fuse or Fatigued Internal Fuse	1	1	1								
Short or Overload on DC Buss in Computer	2	2	2	1							
Shorted Input Rectifiers					1						
Fan Failure in Computer or Excessive Ambient Temperature						1				2	
Faulty Thermostat						2					
One or More Fuses on Rear Panel Blown								1			
Excessively Noisy Electrical Device being used in the Accessory Outlet							3		2		
AC Input Line Too High or on Improper Tap						3					
AC Input Line Too Low or on Improper Tap	4	4	4	2			2		1		
Plug-In P.C. Card has Faulty Component(s)	3	3	3				1		3		
Faulty Key Switch in Computer. Faulty Relay in Power Supply							4			1	1
+17V Fuse Blown				3							

SECTION VI

INSTALLATION

1.0 GENERAL

In selecting a location for the installation of the D-112, factors of major consideration are as follows:

(a) Space
(b) Environment
(c) Power Availability

Choose a location which allows a working area behind as well as in front of the cabinets housing the computer and peripherals. Adequate space allocation enables easy access to the component units, an important factor for ease of maintenance.

Temperature and humidity are important factors in selecting a room for locating the D-112.

The ideal ambient operating temperature in terms of computer life is between 70°F and 85°F (21°C and 30°C). However, operation at temperatures between 50°F and 130°F (10°C and 55°C) does not degrade computer performance.

During shipping and storage the computer can withstand temperature variations between 0°C and 65°C.

The computer will operate in a humidity range of between 10% and 90%.

The room selected should have a 115V ±10V, 60 Hz ±5% source capable of delivering 15 Amperes. The D-112 utilizes 5 Amperes with all mainframe options installed, but provides up to 10 Amperes for peripherals that may be connected through the convenience outlets mounted on the rear panel of the computer.

The power source termination of the D-112 power cable is equipped with a three pronged connector.

The D-112 is electrically connected to peripheral devices by a system of cabling, a portion of which is designated for strictly I/O bus functions while the remainder is designated for what can be referred to as special purpose interconnections.

2.0 INTERFACE CONNECTORS

Figure 6-1 illustrates the connector interface for all signals exiting the main frame. Connectors AØ5, AØ6, BØ3, BØ4, BØ5 and BØ6, are dedicated to the I/O bus proper. The remaining connectors are for special signal requirements as specified by the user.

Signals at the computer side of the connector interface connect to the main frame I/O circuit board by means of internal cabling and the back plane wiring board. Three special purpose Teletype signals are routed from the Teletype Control Logic located on the I/O circuit board to the TTY connector BØ3 on the connector interface. These three signals are routed through the same internal main frame cabling as the I/O bus.

The I/O bus signals and the special purpose signals are transmitted from the connector interface through ribbon type cables which exit the main frame cabinet through a window type opening in the rear of the unit.

2.1 DEVICE CABLE INTERCONNECTION (BASIC POSITIVE BUS)

Figure 6-2 shows the device end of the I/O bus cables and the special purpose TTY cable for the Positive I/O bus provided with the basic computer system. The three cables connecting to BØ4, BØ5 and BØ6 and which carry the I/O bus signals identified with the basic system are routed directly to an external device. The first device, as well as every other device using the basic I/O bus, jumps all the I/O signals to a duplicate connector which passes the basic I/O bus on to the next device. The two cables connecting the AØ5 and AØ6 and which carry I/O bus signals identified with the Data Break Option are routed directly to any single high speed device using this option or, if more than one device is using the option, the cables connect to the Type DM-2 Data Channel Multiplexer. This unit can handle up to three high speed devices.

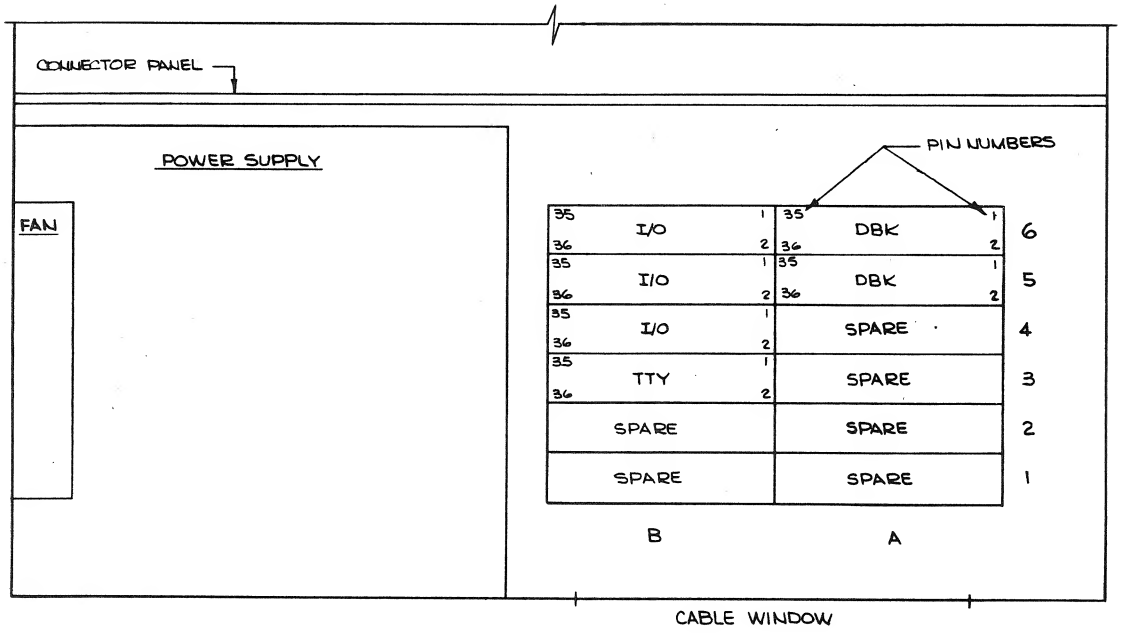
The cable carrying the three special purpose signals from the TTY connector BØ3 are routed directly to the TTY unit.

2.2 DEVICE CABLE INTERCONNECTION (NEGATIVE BUS)

The Type NB-1 negative bus option is provided for users employing negative logic in the external device. When this option is used, a single circuit board in the main frame containing the basic Positive I/O bus is removed and a single circuit board containing the NB-1 bus is installed in the same location. The pin assignments for the I/O transmission cable to the external devices remain the same at the computer end. The I/O transmission cable used with the NB-1, however, terminates in ten single-sided connectors rather than five double-sided connectors as is the case with the basic Positive I/O bus. Figure 6-3 shows the I/O cables used with this option.

2.3 PIN ASSIGNMENTS

Pin assignments by connector are provided in Table 6-1 for the Positive I/O bus and in Table 6-2 for the Negative I/O bus. The D-112 pin designations



TOP VIEW

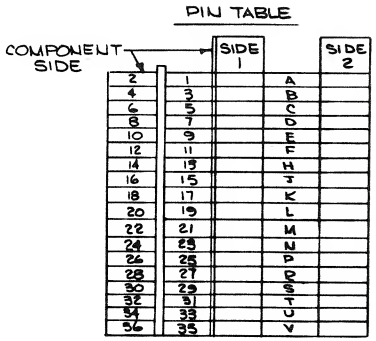


Figure 6-1. Interface Connectors

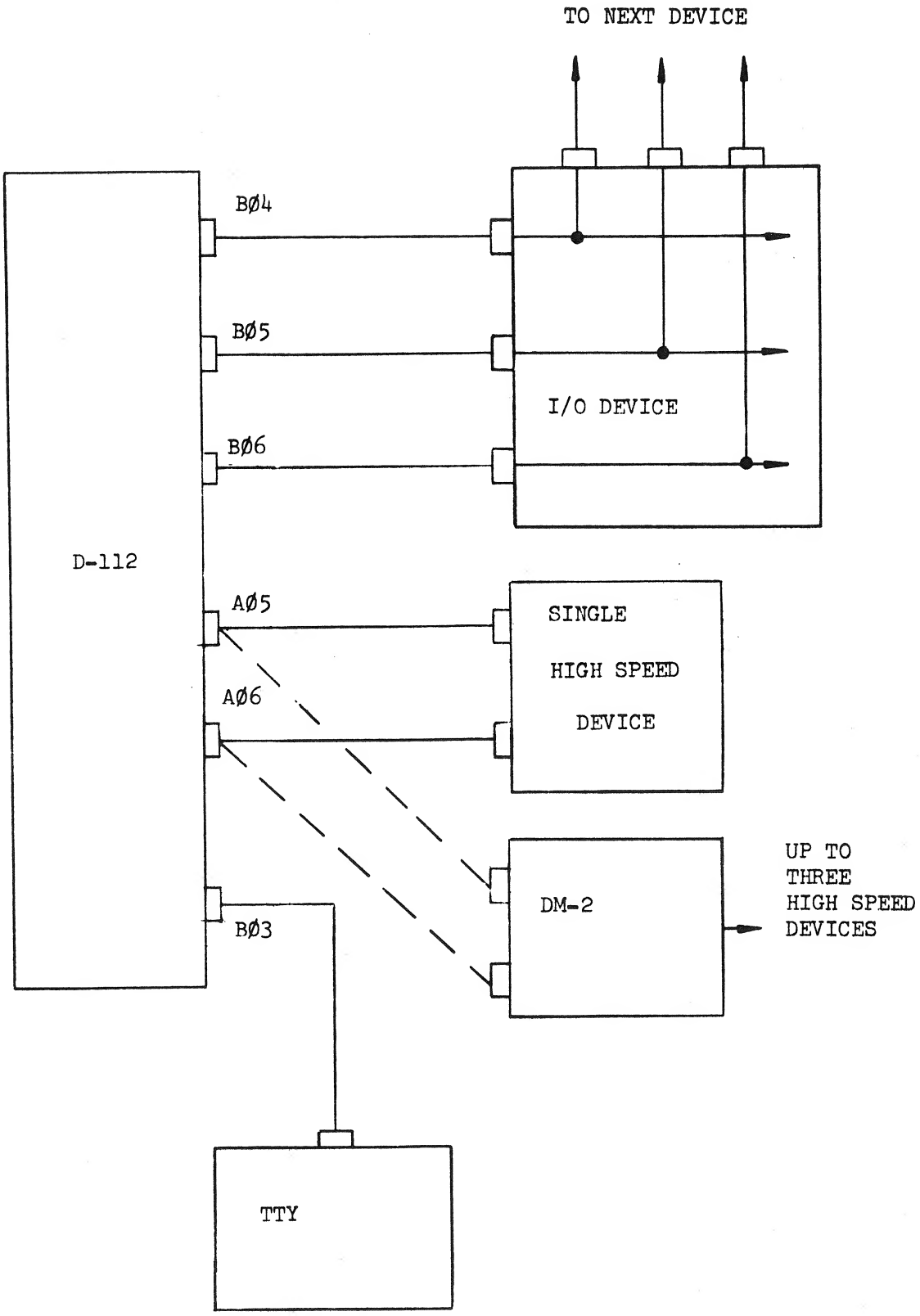


Figure 6-2. Positive Bus Device Cable Interconnection

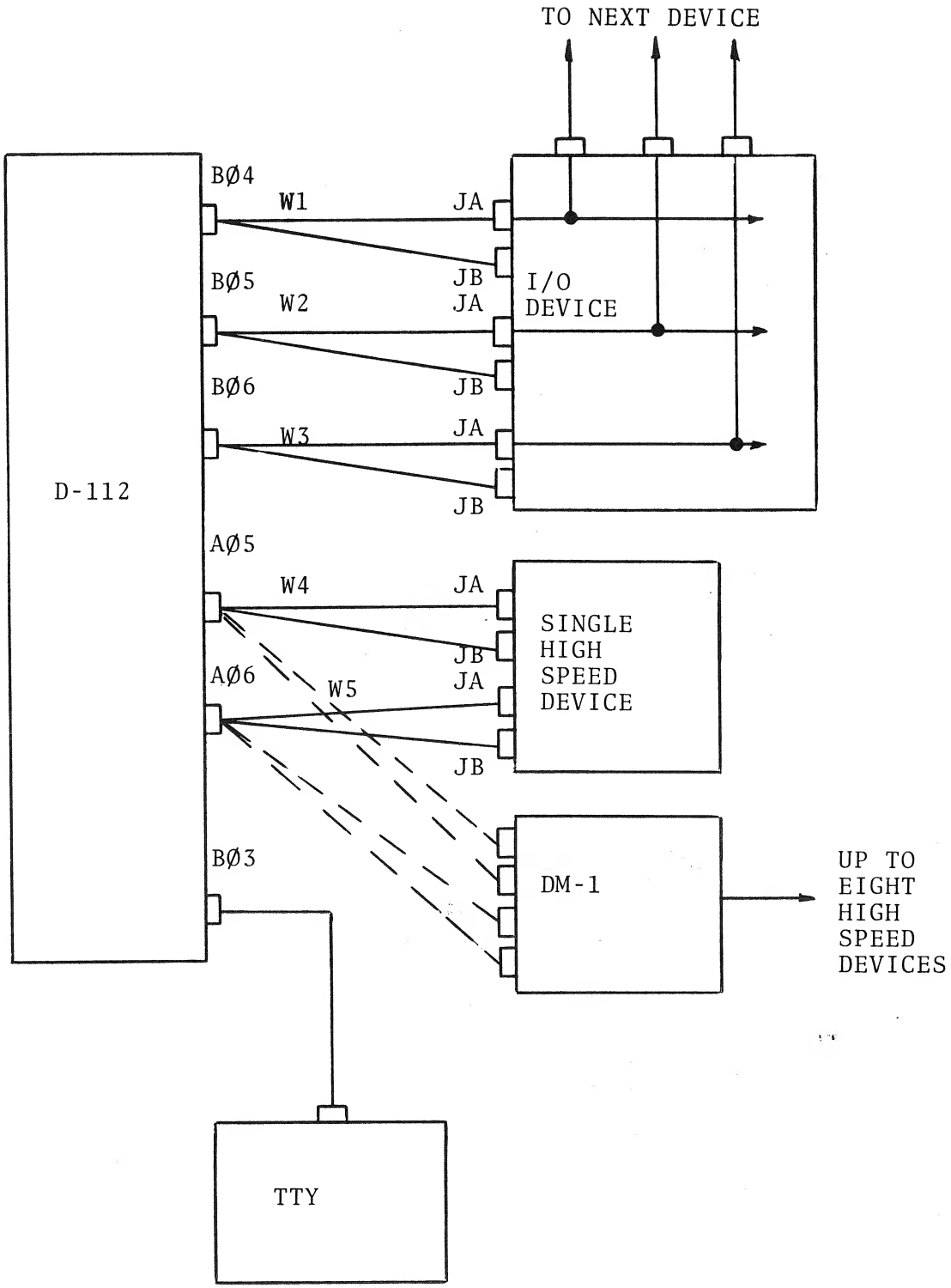


Figure 6-3. Negative Bus Device Cable Interconnection

are given, together with the type of signal and the mnemonic identification of each one. Connector panel assignments are given in Table 6-3.

2.4 TTY CABLE CONNECTION

(Remove the Teletypewriter plastic cover thereby revealing the Teletypewriter power cable and I/O cable which is terminated in a printed circuit board, part no. 400070).

To connect the I/O cable proceed in the following way:

(i) remove the top cover of the chassis.

(ii) unscrew and remove the foam clad bracket located on the chassis back panel.

(iii) insert the cable through the opening being careful not to rip the remaining piece of foam.

(iv) insert the cable connector into the proper connector block slot.

(v) carefully screw the bracket back into place, thereby insuring proper ventilation of the unit while forming a dust shield and support around the cable.

(vi) mount the top cover back in place.

TABLE 6-1. POSITIVE I/O BUS

D-112 PIN	SIGNAL	MNEMONIC	D-112 PIN	SIGNAL	MNEMONIC
	CONNECTOR AØ5			CONNECTOR BØ3	
2	GRD		2		
4	LEVEL	DATA ØØ*	4		
6	GRD		6		
8	LEVEL	DATA Ø1*	8		
10	LEVEL	DATA Ø2*	10		
12	GRD		12		
14	LEVEL	DATA Ø3*	14		
16	LEVEL	DATA Ø4*	16		
18	GRD		18		
20	LEVEL	DATA Ø5*	20		
22	LEVEL	DATA Ø6*	22		
24	GRD		24		
26	LEVEL	DATA Ø7*	26		
28	GRD		28		
30	LEVEL	DATA Ø8*	1	+5VDC	
32	GRD		3	-12VDC	
5	GRD		5	GRD	
7	LEVEL	DATA Ø9*	7		
9	LEVEL	DATA 1Ø*	9		TYLINEIN*
13	LEVEL	DATA 11*	11		
15	GRD		13		TYOUT
17	LEVEL	3 CYCLE*	15		
19	GRD		17		
21	LEVEL	CAINCR	19		
23	GRD		21		TYREAD OUT
25	LEVEL	BWCOVERF*	23		
27	GRD		25		
29	LEVEL	EXTDATA ADD2*	27		
31	LEVEL	EXTDATA ADD1*	29		
33	GRD		31		
35	LEVEL	EXTDATA ADDØ*	33		
			35		
Note data has no *					
	CONNECTOR AØ6			CONNECTOR BØ4	
2	GRD		2	GRD	
4	LEVEL	DATA ADD ØØ*	4	LEVEL	INBUS ØØ*

TABLE 6-1. POSITIVE I/O BUS (Continued)

D-112 PIN	SIGNAL	MNEMONIC
	CONNECTOR BØ4 (Continued)	
6	GRD	
8	LEVEL	INBUS Ø1*
10	LEVEL	INBUS Ø2*
12	GRD	
14	LEVEL	INBUS Ø3*
16	LEVEL	INBUS Ø4*
18	GRD	
20	LEVEL	INBUS Ø5*
22	LEVEL	INBUS Ø6*
24	GRD	
26	LEVEL	INBUS Ø7*
28	GRD	
30	LEVEL	INBUS Ø8*
32	GRD	
5	GRD	
7	LEVEL	INBUS Ø9*
9	LEVEL	INBUS 1Ø*
11	GRD	
13	LEVEL	INBUS 11*
15	GRD	
17	LEVEL	I0 SKIP*
19	GRD	
21	PULSE	INT REQ*
23	GRD	
25	LEVEL	ACCCLEAR*
27	GRD	
29	LEVEL	BRUN*
31		
33	GRD	
35		
	CONNECTOR BØ5	
2	GRD	
4	LEVEL	BMBR ØØ
6	GRD	
8	LEVEL	BMBR Ø1
10	LEVEL	BMBR Ø2
12	GRD	
14	LEVEL	BMBR Ø3*
16	LEVEL	BMBR Ø3
18	GRD	
20	LEVEL	BMBR Ø4*
22	LEVEL	BMBR Ø4
24	GRD	
26	LEVEL	BMBR Ø5*
28	GRD	
30	LEVEL	BMBR Ø5
32	GRD	
5	GRD	
7	LEVEL	BMBR Ø6*
9	LEVEL	BMBR Ø6

D-112 PIN	SIGNAL	MNEMONIC
	CONNECTOR BØ5 (Continued)	
11	GRD	
13	LEVEL	BMBR Ø7*
15	GRD	
17	LEVEL	BMBR Ø7
19	GRD	
21	LEVEL	BMBR Ø8*
23	GRD	
25	LEVEL	BMBR Ø8
27	GRD	
29	LEVEL	BMBR Ø9
31	LEVEL	BMBR 1Ø
33	GRD	
35	LEVEL	BMBR 11
	CONNECTOR BØ6	
2	GRD	
4	LEVEL	I0 ACC ØØ
6	GRD	
8	LEVEL	I0 ACC Ø1
10	LEVEL	I0 ACC Ø2
12	GRD	
14	LEVEL	I0 ACC Ø3
16	LEVEL	I0 ACC Ø4
18	GRD	
20	LEVEL	I0 ACC Ø5
22	LEVEL	I0 ACC Ø6
24	GRD	
26	LEVEL	I0 ACC Ø7
28	GRD	
30	LEVEL	I0 ACC Ø8
32	GRD	
5	GRD	
7	LEVEL	I0 ACC Ø9
9	LEVEL	I0 ACC 10
11	GRD	
13	LEVEL	I0 ACC 11
15	GRD	
17	PULSE	BIOP1
19	GRD	
21	PULSE	BIOP2
23	GRD	
25	PULSE	BIOP4
27	GRD	
29	PULSE	BLT3
31	PULSE	BLT1
33	GRD	
35	PULSE	BINIT1

TABLE 6-2. NEGATIVE I/O BUS

D-112 PIN	SIGNAL	MNEMONIC
	CONNECTOR BØ5	
JA5	GRD	
JA7	LEVEL	BMBRØØ
JA9	LEVEL	BMBRØ1
JA11	GRD	
JA13	LEVEL	BMBRØ2
JA15	GRD	
JA17	LEVEL	BMBRØ3*
JA19	GRD	
JA21	LEVEL	BMBRØ3
JA23	GRD	
JA25	LEVEL	BMBRØ4*
JA27	GRD	
JA29	LEVEL	BMBRØ4
JA31	LEVEL	BMBRØ5*
JA33	GRD	
JA35	LEVEL	BMBRØ5
JB5	GRD	
JB7	LEVEL	BMBRØ6*
JB9	LEVEL	BMBRØ6
JB11	GRD	
JB13	LEVEL	BMBRØ7*
JB15	GRD	
JB17	LEVEL	BMBRØ7
JB19	GRD	
JB21	LEVEL	BMBRØ8*
JB23	GRD	
JB25	LEVEL	BMBRØ8
JB27	GRD	
JB29	LEVEL	BMBRØ9
JB31	LEVEL	BMBR10
JB33	GRD	
JB35	LEVEL	BMBR11
	CONNECTOR BØ6	
JA5	GRD	
JA7	LEVEL	IOACCØ0
JA9	LEVEL	IOACCØ1
JA11	GRD	
JA13	LEVEL	IOACCØ2
JA15	GRD	
JA17	LEVEL	IOACCØ3
JA19	GRD	
JA21	LEVEL	IOACCØ4
JA23	GRD	
JA25	LEVEL	IOACCØ5
JA27	GRD	
JA29	LEVEL	IOACCØ6
JA31	LEVEL	IOACCØ7
JA33	GRD	
JA35	LEVEL	IOACCØ8

D-112 PIN	SIGNAL	MNEMONIC
	CONNECTOR BØ6 (Continued)	
JB5	GRD	
JB7	LEVEL	IOACCØ9
JB9	LEVEL	IOACC10
JB11	GRD	
JB13	LEVEL	IOACC11
JB15	GRD	
JB17	PULSE	BIOP1
JB19	GRD	
JB21	LEVEL	BIOP2
JB23	GRD	
JB25	LEVEL	BIOP4
JB27	GRD	
JB29	LEVEL	BLT3
JB31	LEVEL	BLT1
JB33	GRD	
JB35	PULSE	BINIT
	CONNECTOR BØ3	
2		
4		
6		
8		
10		
12		
14		
16		
18		
20		
22		
24		
26		
28		
1	+5 VDC	
3	-12 VDC	
5	GRD	
7		
9		TYLINEIN*
11		
13		TYOUT
15		
17		
19		
21		TYREADOUT
23		
25		
27		
29		
31		
33		
35		

TABLE 6-2. NEGATIVE I/O BUS (Continued)

D-112 PIN	SIGNAL	MNEMONIC
	CONNECTOR AØ5	
JA5	GRD	
JA7	LEVEL	DATAØØ*
JA9	LEVEL	DATAØ1*
JA11	GRD	
JA13	LEVEL	DATAØ2*
JA15	GRD	
JA17	LEVEL	DATAØ3*
JA19	GRD	
JA21	LEVEL	DATAØ4*
JA23	GRD	
JA25	LEVEL	DATAØ5*
JA27	GRD	
JA29	LEVEL	DATAØ6*
JA31	LEVEL	DATAØ7*
JA33	GRD	
JA35	LEVEL	DATAØ8*
JB5	GRD	
JB7	LEVEL	DATAØ9*
JB9	LEVEL	DATA10*
JB11	GRD	
JB13	LEVEL	DATA11*
JB15	GRD	
JB17	LEVEL	3CYCLE*
JB19	GRD	
JB21	LEVEL	CAINCR
JB23	GRD	
JB25	LEVEL	BCOVERF*
JB27	GRD	
JB29	LEVEL	EXTDATAADD2*
JB31	LEVEL	EXTDATAADD1*
JB33	GRD	
JB35	LEVEL	EXTDATAADDØ*
	CONNECTOR AØ6	
JA5	GRD	
JA7	LEVEL	DATAADDØØ*
JA9	LEVEL	DATAADDØ1*
JA11	GRD	
JA13	LEVEL	DATAADDØ2*
JA15	GRD	
JA17	LEVEL	DATAADDØ3*
JA19	GRD	
JA21	LEVEL	DATAADDØ4*
JA23	GRD	
JA25	LEVEL	DATAADDØ5*
JA27	GRD	
JA29	LEVEL	DATAADDØ6*
JA31	LEVEL	DATAADDØ7*
JA33	GRD	
JA35	LEVEL	DATAADØ8*
JB5	GRD	

D-112 PIN	SIGNAL	MNEMONIC
	CONNECTOR AØ6 (Continued)	
JB7	LEVEL	DATAADDØ9*
JB9	LEVEL	DATAADD10*
JB11	GRD	
JB13	LEVEL	DATAADD11*
JB15	GRD	
JB17	LEVEL	BRKRQSTBUS*
JB19	GRD	
JB21	LEVEL	DATAIN
JB23	GRD	
JB25	LEVEL	BREAK
JB27	GRD	
JB29		BADDACCEP
JB31	LEVEL	MEMINCR*
JB33	GRD	
JB35		
	CONNECTOR BØ4	
JA5	GRD	
JA7	LEVEL	INBUSØØ*
JA9	LEVEL	INBUSØ1*
JA11	GRD	
JA13	LEVEL	INBUSØ2*
JA15	GRD	
JA17	LEVEL	INBUSØ3*
JA19	GRD	
JA21	LEVEL	INBUSØ4*
JA23	GRD	
JA25	LEVEL	INBUSØ5*
JA27	GRD	
JA29	LEVEL	INBUSØ6*
JA31	LEVEL	INBUSØ7*
JA33	GRD	
JA35	LEVEL	INBUSØ8*
JB5	GRD	
JB7	LEVEL	INBUSØ9*
JB9	LEVEL	INBUS10*
JB11	GRD	
JB13	LEVEL	INBUS11*
JB15	GRD	
JB17	LEVEL	I0 SKIP*
JB19	GRD	
JB21	PULSE	INTREQ*
JB23	GRD	
JB25	LEVEL	ACCLEAR*
JB27	GRD	
JB29	LEVEL	BRUN*
JB31		
JB33	GRD	
JB35		

NOTES

A. WARNING

The computer should not be operated if the two foam surfaces in the rear cable port are not reasonably compressed since this adversely affects ventilation of the unit.

B. CHASSIS MOUNTING

Prior to rack-mounting of the chassis, fasten the 2 slides to the sides of the unit by means of the 6 screws contained in a plastic bag.

C. OPTIONAL CABINET EQUIPMENT FOR SYSTEM INSTALLATION

The following cabinet hardware is offered for housing D-112 system components:

Type C-1 Cabinet Relay Rack
Standard 72" x 30" x 19"

Type E-1 Expansion Cabinet with Power Supply
Standard 22" x 19" x 8-3/4"

Type EP-1 End Panel

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS

CU-1

P - 1

	A	B		
	+5	1	GRD	
SP	TY SHFEN	2	GRD	
SP	EXT INTCLR	3	INT CONT	SP MEX
CU-2	DATAEN	4	TYCARRIN	SP
SP	DNOSHF	5	EXMEMEN	EA, SP
SP	TYLSTSHF	6	ME INHØ911	SP
SP	EXINTSET	7	TY INST	SP
SP	EX-INTINH	8	TY RH TSHF	SP
CU-2	LINK-EN	9	LINKEN	CU-2
CU-2	OPI	10		
SP	TYDATA	11		
		12		
CU-2, EA, SP	SLT4	13		
I/O, EA	IOACCØ2	14	XORMBR46	CU-2
I/O, EA	IOACCØ1	15	IOACCØØ	I/O, CU-2, EA
CU-2	MANPRES	16	EABUS11	EA, SP
CU-2	XORMBR57	17	BLINK	CU-2
		18	CARRYOUT	CU-2
		19		
CU-2	PT1	20	MAREN0511	CU-2
EA, SP	EABUSØ1	21	FSET	CU-2
EA, SP	EABUS1Ø	22	EABUSØ4	EA, SP
CU-2	INTEN	23	INTREQ	I/O

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

CU-1

P - 1

		A B		
CU-2	START	24		
		25	ANDEN	CU-2
CU-2	OP1	26	MBRLOAD	CU-2
EA, SP	EABUSØ5	27	EABUSØ9	EA, SP
EA, SP	EABUSØ2	28	EABUSØØ	EA, SP
CU-2	MARENØØØ4	29	EABUSØ8	EA, SP
CU-2	MEMENØØØ4	30	PCENABLE	CU-2
SP	TYLKSHCON	31		
EA, SP	EABUSØ6	32	EABUSØ7	EA, SP
EXMEM	EXMEMCLR	33	EABUSØ3	EA, SP
I/O	DATA ADD Ø9	34	DATA ADD11	I/O
I/O	DATA ADD Ø8	35	DATA ADD1Ø	I/O
I/O	DATA Ø9	36	DATA 11	I/O
I/O	DATA ADD Ø5	37	DATA ADDØ6	I/O
I/O	DATA Ø6	38	DATA 1Ø	I/O
EA, CU-2, I/O, MTC	BUMBRØ8	39	CARRY IN	CU-2
M, CU-2, I/O, EA, MTC	BUMBRØ6	40	BUMBRØ7	CU-2, EA, MTC, I/O
EA, MTC, I/O, CU-2	BUMBRØ4	41	BUMBRØ5	CU-2, EA, MTC, I/O
MTC	BMARØ9	42	BUMRØ3	CU-2, I/O, MTC
MTC	MAR11	43	BMAR10	MTC

CU-1

- P-2 -

CU-2	IOT-BFETCH	1	BUMBRØ1	I/O, MTC
CU-2	ACCSKIP	2	BUMRØØ	I/O, MTC
EA, I/O	10ACCØ9	3	AUTINDADD	CU-2
EA, I/O	10ACC1Ø	4	IOACC11	I/O, EA
CU-2	BFETCH	5	BUMBRØ2	I/O, MTC
I/O	DATAØ5	6	DATA Ø7	I/O
I/O	DATAØ8	7	DATAADDØ7	I/O
EA, I/O	IOACCØ6	8	LT4	CU-2, EA
EA, I/O	IOACCØ7	9	IOACCØ8	I/O, EA
EA, I/O	IOACCØ3	10	IOACCØ4	I/O, EA
CU-2	INT	11	10ACCØ5	I/O, EA
CU-2	CPUIOT	12	INT	CU-2
MTC	BMARØ7	13	BMARØ8	MTC
CU-2, MTC	BMARØØ	14	BMARØ6	MTC
CU-2, MTC	BMARØ2	15	BMARØ1	CU-2, MTC
I/O	IOINBUSØ6	16	BMARØ4	CU-2, MTC
CU-2, MTC	BMARØ3	17	IOINBUS1Ø	I/O

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

CU-1

- P-2 -

	A		B	
I/O, MTC, EA, CU-2	BUMBRØ9	18	BMAR05	MTC
EA, I/O, MTC, CU-2	BUMBR1Ø	19	BUMBR11	CU-2, EA, I/O, MTC
CU-2	$\overline{\text{DATA ADDEN}}$	20		
CU-2	MARLOAD	21		
I/O	IOINBUS11	22	$\overline{\text{ACCEN}}$	CU-2
I/O	IOINBUSØ7	23	IOINBUSØ8	I/O
CU-2	ACCLOAD	24	$\overline{\text{MEMENØ511}}$	CU-2
		25		
CU-2	SREN	26		
I/O	DATAADDØ4	27	PCLOAD	CU-2
I/O	IOINBUSØ9	28	ACCEN	CU-2
I/O	IOINBUSØ2	29	IOINBUSØ4	I/O
I/O	DATA04	30	IOINBUSØ5	I/O
I/O	DATAADDØ2	31	DATAADDØ3	I/O
I/O	DATAADDØØ	32	DATAADDØ1	I/O
I/O	DATAØ2	33	DATAØ3	I/O
I/O	DATAØØ	34	DATAØ1	I/O
I/O	IOINBUSØ1	35	$\overline{\text{IOINBUSEN}}$	I/O
I/O	IOINBUSØ3	36	IOINBUSØØ	I/O
MTC, EA	MEMØ9	37	MEM1Ø	MTC, EA
MTC, EA	MEMØ7	38	MEMØ8	MTC, EA
MTC, EA	MEMØ5	39	MEMØ6	MTC, EA
CU-2, MTC, EA	MEMØ2	40	MEMØ4	MTC, EA
MTC, EA	MEM11	41	MEMØ1	CU-2, MTC, EA
MTC, EA	MEMØ3	42	MEMØØ	CU-2, MTC, EA
	+5 Volts	43	GRD	

CU-2

- P1 -

	+5	1	GRD	
M-EX, SP	$\overline{\text{RESTART}}$	2	$\overline{\text{BUFF}}$	M-EX, SP
SP	$\overline{\text{IOPCEN}}$	3	$\overline{\text{EMA}}$	SP
CU-1	$\overline{\text{DATA-EN}}$	4	$\overline{\text{EAPCEN}}$	EA
EA	EA-ENMEM	5	$\overline{\text{BRKRQST}}$	I/O
EA	$\overline{\text{EA-RUN}}$	6	$\overline{\text{EAIRCLR}}$	EA
I/O	3 Cycle	7	DATAIN	I/O
SP	$\overline{\text{STORE}}$	8	MEMINC	I/O
CU-1	$\overline{\text{LINK-EN}}$	9	LINKEN	CU-1
CU-1	$\overline{\text{OP1}}$	10	$\overline{\text{EAENACCL}}$	EA
EA	$\overline{\text{EAEND}}$	11	$\overline{\text{EAENACC}}$	EA

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

CU-2

- P1 -

		A B		
EA	EASTART	12	TYSET	SP
CU-1, SP, EA	SLT4	13	ADDACCEP	I/O
I/O	BWCOVERF	14	XORMBR46	CU-1
EA	OPR	15	IOACCØØ	CU-1
CU-1, M-EX	MANPRES	16	DWCSET	M-EXT
CU-1	XORMBR57	17	BLINK	CU-1
EA, SP, M-EX	PT3	18	CARRYOUT	CU-1
EA, SP, M-EX	PT2	19	BEXECUTE	EA, M-EX, SP
CU-1, SP, M-EX	PT1	20	MARENØ511	CU-1
EA	PT2	21	FSET	CU-1, M-EX
	BREAK OK	22	PT3	SP, EA
CU-1	INTEN	23	PIOT	M-EX
CU-1	START	24	JMS	M-EX
EA	EAESET	25	ANDEN	CU-1
CU-1	OP1	26	MBRLOAD	CU-1
EA, M-EX, SP	BFETCH	27	PT4	SP, M-EX, EA
M-EX	DDCSET	28		
CU-1	MARENØØØ4	29	ESET	M-EX
CU-1	MEMENØØØ4	30	PCENABLE	CU-1
	DSET	31		
M-TC	WRITE START	32	READ START	M-TC
M-EX	JMP	33	LT2	SP, EA
EA, I/O	BRUN	34	DCA	
SP	PC STEP	35	POWERCLR	EA, SP
	TAD	36	AND	
SP	TIMEOK	37		
M-EX	BDWC	38	POWER OK	SP
CU-1, M-EX	BUMBRØ8	39	CARRYIN	CU-1
CU-1, M-EX	BUMBRØ6	40	BUMBRØ7	CU-1, M-EX
CU-1, M-EX	BUMBRØ4	41	BUMBRØ5	CU-1, M-EX
I/O	BDDC	42	BUMBRØ3	CU-1, M-EX
M-EX, SP	BDEFER	43	BLM2	EA, SP, M-EX

CU-2

P2

CU-1	IOTBFETCH	1	BLT3	SP, EA
CU-1	ACCSKIP	2	TLT1	SP, EA, M-EX
SP, M-Ex, EA	PM2	3	AUTINDADD	CU-1
M-EX	KDEPKEXKST	4	CLK2	
CU-1	BFETCH	5	IOT	M-EX

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

MEM TIMING CONT. (MTC)

- P1 -

		A	B		
	+5V	1		+5V	
	+12V	2		+12V	
CU-2	WRITE START	3		(INH RES14)	MSTACK
	ZONE Ø	4		(INH RES 16)	MSTACK
	RMW	5		INH RES Ø6	MSTACK
	ZONE 1	6		INH RES 11	MSTACK
	GRD	7		INH RES Ø8	MSTACK
CU-2	READ START	8		ADD LTCH-ALØ	MSTACK
	(MBR16)	9		ADD LTCH-AL1	MSTACK
CU-1	BUMBRØ8	10		ADD LTCH-AL2	MSTACK
	(MBR15)	11		(INH RES 15)	MSTACK
	GRD	12		(INH RES 17)	MSTACK
CU-1	BUMBRØ7	13		INH RES Ø7	MSTACK
	(MBR17)	14		INH RESØ9	MSTACK
CU-1	BUMBRØ6	15		INH RES1Ø	MSTACK
CU-1, SP	MEMØ6	16		INH DRIVEØ6	MSTACK
	GRD	17		INH DRIVE 11	MSTACK
	(MEM 15)	18		(INH DRIVE 16)	MSTACK
	(MEM 17)	19		INH DRIVE Ø8	MSTACK
CU-1, SP	MEM Ø7	20		(INH DRIVE 14)	MSTACK
CU-1, SP	MEM Ø8	21		(INH DRIVE 15)	MSTACK
	GRD	22		INH DRIVE Ø9	MSTACK
	(MEM 16)	23		INH DRIVE 1Ø	MSTACK
	READ (OPT)	24		WRITE TIMING	MSTACK
	END OF CYCLE	25		READ TIMING	MSTACK
	MEM BUSY	26		SENSE AMP IN BIT 1Ø	MSTACK
	GRD	27		SENSE AMP IN BIT 11	MSTACK
CU-1	BUMBR 1Ø	28		SENSE AMP IN BIT 8	MSTACK
SP	MBR 12	29		SENSE AMP IN BIT 9	MSTACK
CU-1	BUMBRØ9	30		SENSE AMP IN BIT 6	MSTACK
	(MBR 13)	31		SENSE AMP IN BIT 7	MSTACK
CU-1	BUMBR 11	32		GRD	
	(MBR14)	33		ZONE Ø READ EN	MSTACK
	DATA AVAIL	34		SENSE AMP STROBE	MSTACK
	WRITE (OPT)	35		ZONE 1 READ EN	MSTACK
	INHIBIT (OPT)	36		INH TIMING	MSTACK
	(MEM 13)	37		(SENSE AMP IN BIT 15)	MSTACK
	(MEM 14)	38		(SENSE AMP IN BIT 14)	MSTACK
SP	MEM 12	39		(SENSE AMP IN BIT 13)	MSTACK
CU-1, SP	MEM 1Ø	40		(SENSE AMP IN BIT 17)	MSTACK

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

CU-2

P2

		A	B		
M-EX	KLA	6			
EA, SP, M-EX	PM3	7		LT3	EA, Sp, M-EX
I/O	IOSKIP	8		LT4	CU-1, EA
M-EX	OP2	9		IOCLOCK	
M-EX	PT4	10		IOENABLE	I/O
CU-1	INT	11		DBK MEMINC	
CU-1	CPUIOT	12		INT	CU-1, M-EX
I/O	IOP2	13		PM1	Sp, EA, M-EX
CU-1	BMARØØ	14		IOP4	I/O
CU-1	BMARØ2	15		BMARØ1	CU-1
SP	PIOEND	16		BMARØ4	CU-1
CU-1	BMARØ3	17		IOP1	I/O
CU-1, M-EX	BUMBRØ9	18		EXIOPCLK	SP
CU-1, M-EX	BUMBR1Ø	19		BUMBR11	CU-1, M-EX
CU-1	DATA ADDEN	20		LEDR2	M-EX
CU-1	MARLOAD	21		LEDR1	M-EX
M-EX	LEDRØ	22		ACCEN	CU-1
EA	BPAUSE	23		LEIR2	M-EX
CU-1	ACCLOAD	24		MEMENØ511	CU-1
M-EX	LEIRØ	25		LEIRI	M-EX
CU-1	SREN	26		EDSWR2	M-EX
M-EX	EDSWR1	27		PCLOAD	CU-1
M-EX	EDSWRØ	28		ACCEN	CU-1
M-EX	EISWR2	29		PAR	SP
M-EX	EISWRØ	30		EISWR1	M-EX
SP	TYDISL	31		IOACCCLR	I/O
SP	EXIOINH	32		CLEAR	EA, I/O, M-EX
SP	EXIOEND	33		EAEXECUTE	EA
SP	TYACCLD	30		TSKIP	M-EX
M-EX	MEMEXTIOT	35		TYCYCLE	SP
EA	EALDACC	36		TYINST	SP
EA	EADISL	37		EXPAUSE	SP
SP	EXIOCLK	38		MEACCLD	M-EX
SP	TYINC	39		TYCARRY IN	SP
CU-1	MEMØ2	40		IOPCLD	SP
M-EX, SP	EXIOEN	41		MEMØ1	CU-1
I/O	CAINC	42		MEMØØ	CU-1
	+5 V	43		GRD	

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

MEM TIMING CONT. (MTC)

- P1 -

		A	B		
CU-1 SP	MEM Ø9	41		(SENSE AMP IN BIT 16)	MSTACK
CU-1 SP	MEM 11	42		GRD	
	GRD	43		GRD	

MEM TIMING CONT

- P2 -

	GRD	1		GRD	
	-5V	2		-5V	
CU-1	BMARØ8	3		$\overline{DG}$	MSTACK
	(MAR12)	4		TEST DATA CONTROL	
CU-1	BMAR11	5			
CU-1	BMARØ9	6		GRD	
CU-1	BMAR1Ø	7		(SENSE AMP IN BIT 12)	MSTACK
	LOGIC RESET	8		SENSE AMP IN BIT Ø3	MSTACK
CU-1	BMARØ7	9		SENSE AMP IN BIT Ø2	MSTACK
CU-1	BUMBRØ1	10		SENSE AMP IN BIT Ø1	MSTACK
	GRD	11		SENSE AMP IN BIT Ø4	MSTACK
CU-1	BMARØ4	12		SENSE AMP IN BIT Ø5	MSTACK
CU-1	BMARØ5	13		SENSE AMP IN BIT ØØ	MSTACK
CU-1	BMARØ6	14		ADD LTCH -AL3	MSTACK
CU-1	BMARØ2	15		ADD LTCH AL4	MSTACK
	GRD	16		ADD LTCH AL5	MSTACK
CU-1	BMARØ1	17		ADD LTCH AL6	MSTACK
CU-1	BMARØØ	18		ADD LTCH AL7	MSTACK
CU-1	BMARØ3	19		ADD LTCH AL8	MSTACK
CU-1	BUMBRØ4	20		GRD	
CU-1	BUMBRØ2	21		(INH DRIVE 17)	MSTACK
CU-1	BUMBRØ5	22		INH DRIVE Ø7	MSTACK
CU-1	BUMBRØ3	23		(INH DRIVE 13)	MSTACK
CU-1	BUMBRØØ	24		INH DRIVE Ø5	MSTACK
CU-1, SP	MEMØ4	25		INH DRIVE Ø3	MSTACK
	GRD	26		INH DRIVE ØØ	MSTACK
	+12V	27		+12V	
CU-1, SP	MEMØ2	28		ADD LTCH-AL1Ø	MSTACK
CU-1, SP	MEMØØ	29		ADD LTCH-AL11	MSTACK
CU-1, SP	MEMØ5	30		ADD LTCH-AL9	MSTACK
	(MAR13)	31		INH RES ØØ	MSTACK
CU-1, SP	MEMØ3	32		INH RES Ø3	MSTACK
	(MAR14)	33		INH RES Ø5	MSTACK

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

MEM TIMING CONT

- P2 -

		A	B	
CU-1 SP	MEM Ø1	34	INH DRIVE Ø2	MSTACK
	STACK SELECT 8K	35	INH DRIVE Ø4	MSTACK
	STACK SELECT 4K	36	INH DRIVE Ø1	MSTACK
	STACK SELECT 16K	37	(INH DRIVE 12)	MSTACK
	STACK SELECT 12K	38	INH RES Ø1	MSTACK
	STACK SELECT 2ØK	39	INH RES Ø2	MSTACK
	STACK SELECT 24K	40	INH RES Ø4	MSTACK
	STACK SELECT 32K	41	(INH RES 12)	MSTACK
	STACK SELECT 28K	42	(INH RES 13)	MSTACK
	+5V	43	+5V	

MEM STACK (MST)

- P1 -

+5V	1	+5V	
+12V	2	+12V	
GRD	3	(INH RES 14)	MTC
GRD	4	(INH RES 16)	MTC
GRD	5	INH RES - Ø6	MTC
GRD	6	INH RES -11	MTC
GRD	7	INH RES -Ø8	MTC
GRD	8	ADD LTCH - ALØ	MTC
GRD	9	ADD LTCH - AL1	MTC
GRD	10	ADD LTCH - AL2	MTC
GRD	11	(INH RES 15)	MTC
GRD	12	(INH RES 17)	MTC
GRD	13	INH RES -Ø7	MTC
GRD	14	INH RES -Ø9	MTC
GRD	15	INH RES 1Ø	MTC
GRD	16	INH DRIVE Ø6	MTC
GRD	17	INH DRIVE-11	MTC
GRD	18	(INH DRIVE 16)	MTC
GRD	19	INH DRIVE Ø8	MTC
GRD	20	(INH DRIVE 14)	MTC
GRD	21	(INH DRIVE 15)	MTC
GRD	22	INH DRIVE Ø9	MTC
GRD	23	INH-DRIVE 1Ø	MTC
GRD	24	WRITE TIMING	MTC
GRD	25	READ TIMING	MTC
GRD	26	SENSE AMP IN BIT 1Ø	MTC
GRD	27	SENSE AMP IN BIT 11	MTC

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

MEM STACK (MST)

- P1 -

	A	B		
GRD	28		SENSE AMP IN BIT Ø8	MTC
GRD	29		SENSE AMP IN BIT Ø9	MTC
GRD	30		SENSE AMP IN BIT Ø6	MTC
GRD	31		SENSE AMP IN BIT Ø7	MTC
GRD	32		FIELD "X" (see note 1)	
GRD	33		ZONE Ø READEN	MTC
GRD	34		SENSE AMP STROBE	MTC
GRD	35		ZONE READ EN	MTC
GRD	36		INH TIMING	MTC
GRD	37		(SENSE AMP IN BIT 15)	MTC
GRD	38		(SENSE AMP IN BIT 14)	MTC
GRD	39		(SENSE AMP IN BIT 13)	MTC
GRD	40		(SENSE AMP IN BIT 17)	MTC
GRD	41		(SENSE AMP IN BIT 16)	MTC
-12V	42		-12V	
GRD	43		GRD	

NOTE 1: FIELD X SIGNAL IS CONNECTED TO THE MEX PCB. THE POSITION OF THE STACK DETERMINES WHICH OF THE MEX SIGNALS (FIELD Ø - FIELD 7) IS CONNECTED.

MEM STACK

- P2 -

GRD	1	GRD	
-5V	2	-5V	
GRD	3	DATA GUARD/RESET	MTC
GRD	4		
GRD	5		
GRD	6		
GRD	7	(SENSE AMP IN BIT 12)	MTC
GRD	8	SENSE AMP IN BIT Ø3	MTC
GRD	9	SENSE AMP IN BIT Ø2	MTC
GRD	10	SENSE AMP IN BIT Ø1	MTC
GRD	11	SENSE AMP IN BIT Ø4	MTC
GRD	12	SENSE AMP IN BIT Ø5	MTC
GRD	13	SENSE AMP IN BIT ØØ	MTC
GRD	14	ADD LTCH - AL3	MTC
GRD	15	ADD LTCH - AL4	MTC
GRD	16	ADD LTCH - AL5	MTC
GRD	17	ADD LTCH - AL6	MTC
GRD	18	ADD LTCH - AL7	MTC
GRD	19	ADD LTCH - AL8	MTC

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

MEM STACK

- P2 -

	A	B		
GRD	20			
GRD	21		(INH DRIVE 17)	MTC
GRD	22		INH DRIVE Ø7	MTC
GRD	23		(INH DRIVE 13)	MTC
GRD	24		INH DRIVE Ø5	MTC
GRD	25		INH DRIVE Ø3	MTC
GRD	26		INH DRIVE ØØ	MTC
+12 VOLTS	27		+12 Volts	
GRD	28		ADD LTCH AL1Ø	MTC
GRD	29		ADD LTCH AL 11	MTC
GRD	30		ADD LTCH AL 9	MTC
GRD	31		INH RES ØØ	MTC
GRD	32		IN RES Ø3	MTC
GRD	33		INH RES Ø5	MTC
GRD	34		INH DRIVE Ø2	MTC
GRD	35		INH DRIVE Ø4	MTC
GRD	36		INH DRIVE Ø1	MTC
GRD	37		(INH DRIVE 12)	MTC
GRD	38		INH RES Ø1	MTC
GRD	39		INH RES Ø2	MTC
GRD	40		INH RES Ø4	MTC
GRD	41		(INH RES 12)	MTC
GRD	42		(INH RES 13)	MTC
+5Volts	43		+5 Volts	

MEMEX

- P1 -

	+5V		GRD	
CU-2	$\overline{\text{RESTART}}$	1	$\overline{\text{BUFF}}$	CU-2
		3		
		4		
		5		
		6		
		7	$\overline{\text{EBF SET}}$	
		8	MECLK	
		9		
		10	$\overline{\text{INT INT REQ}}$	I/O
I/O	$\overline{\text{INT I/O Ø7}}$	11	$\overline{\text{EIR SET}}$	
		12	$\overline{\text{EDF SET}}$	
		13	TS INTCLK	

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

MEMEX

- P1 -

	A		B	
		14		
		15		
CU-2	MAN-PRES	16	DWC SET	CU-2
		17	INT I/O Ø6	I/O
CU-2	PT3	18	MEDDADD2	I/O
CU-2	PT2	19	BEXECUTE	CU-2
CU-2	PT1	20	UBF-SET	
		21	FSET	CU-2
		22	UBF CLK	
I/O	MEDDADD1	23	TS PR	
I/O	MEDDADDØ	24	JMS	CU-2
		25	TS IO SHLT	
		26	TS SKIP CK	
CU-2	BFETCH	27	PT4	CU-2
CU-2	DDC SET	28	FDECØ	
	EBFCLK	29	ESET	CU-2
	FDEC1	30	FDEC2	
	EIBCLK	31	INCONT	CU-1
STACK 0, SP	FIELD Ø	32	FIELD 1	STACK 1, SP
CU-1	EXMEMCLR	33	PIOT	CU-2
STACK 2, SP	FIELD 2	34	JMP	CU-2
STACK 3, SP	FIELD 3	35		
STACK 4, SP	FIELD 4	36		
STACK 5, SP	FIELD 5	37	FIELD 6	STACK 6, SP
CU-2	BDWC	38		
CU-2	BUMBRØ8	39	FIELD 7	STACK 7, SP
CU-2	BUMBRØ6	40	BUMBR Ø7	CU-2
CU-2	BUMBRØ4	41	BUMBR Ø5	CU-2
	EDR CLK	42	BUMBR Ø3	CU-2
CU-2	BDEFER	43	BLM2	CU-2

MEM EX

P 2

	DI2	1	EX ADD SREN	
	TLT 1	2	DIØ	
CU-2	PM2	3	EXSWREN	
CU-2	KDEPKEX KST	4	EIB-MBR-EN	
CU-2	LEIRØ	5	IOT	CU-2
CU-2	KLA	6	EDR-MBREN	
CU-2	PM3	7	LT3	CU-2

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

MEM EX

P 2

		A	B		
		8		EXMEIOINH	SP
CU-2	OP2	9		DD2	
CU-2	$\overline{\text{PT4}}$	10		DI1	
		11		TEST 2	
	TEST 1	12		INT	CU-2
		13		PM1	CU-2
		14			
		15			
		16		DDØ	
		17			
		18			
CU-2	BUMBR1Ø	19		BUMBR11	CU-2
I/O	$\overline{\text{INT I/O 1}}$	20		LEDR2	CU-2
		21		LEDR1	CU-2
CU-2	LEDRØ	22			
		23		LEIR2	CU-2
		24			
I/O	$\overline{\text{INT I/O 4}}$	25		LEIR1	CU-2
I/O	$\overline{\text{INT I/O 2}}$	26		EDSWR2	CU-2
CU-2	EDSWR1	27		$\overline{\text{INT I/O 5}}$	I/O
CU-2	EISWRØ	28		BF-6224	
CU-2	EISWR2	29		BF-6214	
CU-2	EISWRØ	30		EISWR1	CU-2
		31			
	$\overline{\text{CLEAR}}$	32		BUMBRØ9	CU-2
		33			
		34		$\overline{\text{TSSKIP}}$	CU-2
CU-2	$\overline{\text{MEMEXTIOT}}$	35			
		36		EIR-CLK	
I/O	$\overline{\text{INT I/O 3}}$	37			
		38		$\overline{\text{MEACCLD}}$	CU-2
		39			
		40		BF-6234	
CU-2	$\overline{\text{EXIOEN}}$	41			
	+5V	42		GRD	
	+5V	43		GRD	

I/O BOARD POSITIVE/NEGATIVE

P1

	+5Volts	1		GRD	
	$\overline{\text{BREAKRQSTBUS}}$	2		$\overline{\text{BRK RQST}}$	CU-2

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

I/O BOARD POSITIVE/NEGATIVE

P1

		A	B		
	+12V	3		BADD ACCEP	
CU-2	3 Cycle	4		DATAIN	CU-2
	INT I/Ø9	5		MEM INC	CU-2
	INBUS Ø9	6		DATA IN	
	INT I/Ø8	7		IN BUS Ø8	
	INT REQ	8		INT INTREQ	M-EX
M-EX	INT I/O 7	9		INBUS Ø7	
	INT I/O 1Ø	10		EXT DATA ADD2	
	IN BUS 1Ø	11		ADDACCEP	CU-2
CU-1	IOACCØ2	12		BWCOVERF	CU-2
	IN BUS 11	13		INT IO 11	
CU-1	IO ACC Ø1	14		IO ACC ØØ	CU-1
	IO ACCOI	15		3 CYCLE	
	IO SKIP	16		IN IO SKIP	
	INBUS Ø6	17		INT I/O 6	M-EX
	LT3	18		MEMINCR	
	+ .6V	19		ME DDADD2	M-EX
	TLT1	20		BMBR07	
	BWCOVEF	21		IO ACCØ2	
	EX DATA ADDØ	22		BMBRØ8	
	EX DATA ADD 1	23		BMBRØ6	
	DATA ADD11	24		INTREQ	CU-1
M-EX	MEDDADD 1	25		IOCLEAR (I/O Pos. Only)	
M-EX	MEDDADD Ø	26		BLT3	
	LD BFF	27		WAIT CONT	
	DATAADD1Ø	28		BUSY	
	BMBR Ø6	29		BMBRØ4	
	DATAADDØ8	30		BMBRØ8	
	DATAADDØ9	31		BMBRØ7	
	TYLINEIN	32		IOACC ØØ	
	BINIT 1	33		REFVOLT	
	BIOP4	34		BMBR04	
	BRUN	35		BMBRØ5	
	DATAADDØ6	36		BMBRØ3	
CU-2	BRUN	37		DATAADD11	CU-1
CU-1	DATA ADD Ø9	38		DATA11	
	DATA09	39		BLT1	
CU-1	DATAADDØ8	40		DATAADD1Ø	CU-1
CU-1	DATAØ9	41		DATA11	CU-1
CU-1	DATAADDØ5	42		DATAADDØ6	CU-1

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

I/O BOARD POSITIVE/NEGATIVE

P1

		A	B	
	$\overline{\text{DATA1Ø}}$	43	$\overline{\text{DATAADDØ5}}$	
CU-1	DATAØ6	44	DATA1Ø	CU-1
CU-1	BUMBRØ8	45	$\overline{\text{DATA06}}$	
CU-1	BUMBRØ6	46	BUMBRØ7	CU-1
CU-1	BUMBRØ4	47	BMBRØ3	
	BMBRØ5	48	BUMBRØ5	CU-1
CU-2	BDDC	49	$\overline{\text{BREAK}}$	
	-12V	50	BUMBRØ3	CU-1

I/O BOARD POS/NEG

- P2 -

	IOACC1Ø	1	BUMBRØ1	CU-1
	IOACCØ6	2	BUMBRØØ	CU-1
	IOACCØ5	3	BMBRØØ	
CU-1	$\overline{\text{IOACCØ9}}$	4	BMBRØ1	
CU-1	$\overline{\text{IOACC1Ø}}$	5	$\overline{\text{IOACC11}}$	CU-1
	IOACC11	6	BUMBRØ2	CU-1
	IOACCØ9	7	BIOP1	
CU-1	DATA Ø5	8	DATA Ø7	CU-1
CU-1	DATA Ø8	9	DATA ADD Ø7	CU-1
CU-1	$\overline{\text{IOACCØ6}}$	10	IO SKIP	CU-2
	BMBRØ2	11	BMBRØ9	
CU-1	$\overline{\text{IOACCØ7}}$	12	$\overline{\text{IOACCØ8}}$	CU-1
CU-1	$\overline{\text{IOACCØ3}}$	13	$\overline{\text{IOACCØ4}}$	CU-1
CU-2	IO ENABLE	14	$\overline{\text{IOACCØ5}}$	CU-1
	BIOP2	15	IOACCØ4	
	BINIT2(IO POS ONLY)	16	IOACCØ8	
CU-2	$\overline{\text{IOP2}}$	17	IOACCØ7	
	$\overline{\text{DATAØ8}}$	18	$\overline{\text{IOP4}}$	CU-2
	$\overline{\text{DATAØ5}}$	19	IOACCØ3	
CU-1	IOINBUSØ6	20	BMBR1Ø	
	$\overline{\text{DATA ADDØ1}}$	21	BMBR11	
CU-2	$\overline{\text{IOP1}}$	22	IOIN BUS 1Ø	CU-1
CU-1	BUMBRØ9	23	$\overline{\text{CLEAR}}$	CU-2
CU-1	BUMBR1Ø	24	BUMBR11	CU-1
	$\overline{\text{DATA ADDØ4}}$	25	$\overline{\text{DATAØ7}}$	
M-EX	INT I/O 1	26	$\overline{\text{CAINCR}}$	
	$\overline{\text{INBUS01}}$	27	$\overline{\text{DATA ADD07}}$	
CU-1	IOINBUS11	28	$\overline{\text{DATA ADDØ3}}$	
CU-1	IOINBUSØ7	29	IOINBUSØ8	CU-1
	$\overline{\text{IN ACC CLEAR}}$	30	$\overline{\text{DATAØ4}}$	

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

I/O BOARD POS/NEG

- P2 -

		A	B	
	ACCCLEAR	31	DATAØ1	
	IN BUS04	32	DATAADDØ2	
M-EX	INT I/O 4	33	DATAADDØØ	
M-EX	INT I/O Ø2	34	INBUSØ5	
CU-1	DATA ADDØ4	35	INT I/O 5	M-EX
CU-1	IOIN BUS Ø9	36	DATAØ3	
CU-1	IOIN BUS Ø2	37	IOINBUS Ø4	CU-1
CU-1	DATA Ø4	38	IOINBUSØ5	CU-1
	INBUS02	39	IOACCCLEAR	CU-2
CU-1	DATA ADDØ2	40	DATA ADDØ3	CU-1
CU-1	DATA ADDØØ	41	DATA ADDØ1	CU-1
CU-1	DATA Ø2	42	DATA Ø3	CU-1
	DATAØØ	43	DATA Ø2	
CU-1	DATAØØ	44	DATA Ø1	CU-1
CU-1	IOINBUSØ1	45	IOINBUSEN	CU-1
CU-1	IOINBUSØ3	46	IOINBUSØØ	CU-1
	INBUS03	47	EXIOINH	
M-EX	INT I/O Ø3	48	INT I/O Ø	
CU-2	CAINC	49	INBUSØØ	
	TYOUT	50	TY READ OUT	
		I/O SPARE		

- P1 -

	+5Volts	1	GRD	
CU-2	EMA	2	RESTART	CU-2
	+12V	3	+12V	
CU-1	TY SHFEN	4	IOPCEN	CU-2
		5		
	3 VOLTS AC	6	EXT INT CLR	CU-1
		7	DNO SHF	CU-1
CU-1	TY CARR IN	8	TYLST SHF	CU-1
		9	MEINHØ911	CU-1
		10	EX INT SET	CU-1
		11	TYINST	CU-1
CU-1	EX-INT-INH	12	SLT4	CU-1, CU2, EA
		13	TYRHT SHF	CU-1
		14	STORE	CU-2
		15	TY DATA	CU-1
CU-1	EABUS11	16	TY SET	CU-2
		17	EXMEMEN	CU-1
MEM-EX	FIELD 3	18	PT3	CU-1

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

I/O SPARE

- P1 -

	A	B	
	19	B EXECUTE	CU-2
CU-2 PT2	20	PT1	CU-1
	21	$\overline{\text{BUFF}}$	CU-2
	22	$\overline{\text{EABUSØ1}}$	CU-1
CU-2 PT3	23		
	24	$\overline{\text{EABUSØ4}}$	CU-1
	25	$\overline{\text{EABUS1Ø}}$	CU-1
	26	FIELD 1	M-EX
CU-1 $\overline{\text{EABUSØ9}}$	27	PT4	CU-2
CU-1 $\overline{\text{EABUSØ5}}$	28	FIELD2	M-EX
CU-2 BFETCH	29		
	30	$\overline{\text{EABUSØ2}}$	CU-1
GRD	31	$\overline{\text{EABUSØØ}}$	CU-1
GRD	32	$\overline{\text{EABUSØ8}}$	CU-1
CU-1 $\overline{\text{TY LK SH CON}}$	33		
CU-1 $\overline{\text{EABUSØ7}}$	34		
CU-2 PCSTEP	35	MBR12	MTC
CU-1 $\overline{\text{EABUSØ6}}$	36	$\overline{\text{INTCONT}}$	CU-1
CU-1 $\overline{\text{EABUSØ3}}$	37		
CU-2 LT2	38	FIELD Ø	M-EX
	39		
	40	$\overline{\text{POWER CLR}}$	CU-2
	41		
	42	FIELD 6	M-EX
CU-2 TIME OK	43	MEM 12	MTC
CU-2 $\overline{\text{POWER OK}}$	44	FIELD 7	M-EX
	45	FIELD 4	M-EX
	46		
CU-2 BDEFER	47	FIELD 5	M-EX
	48	BLM2	CU-2
	49		
-12V	50		

I/O SPARE

- P2 -

1	3 VAC	
2	$\overline{\text{BLT3}}$	CU-2
3	TLT1	CU-2
4	PM2	CU-2
5		
6		

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

I/O SPARE

- P2 -

		A B		
		7		
		8		
		9	LT3	CU-2
		10	PM3	CU-2
		11	EXMEIONH	MEM-EX
		12	GRD	
		13		
		14		
		15		
		16		
		17		
		18		
		19		
		20	PM1	CU-2
		21		
		22		
		23		
		24	$\overline{\text{EXIOPCLK}}$	CU-2
		25		
		26		
		27	$\overline{\text{PIOEND}}$	CU-2
		28		
		29		
		30		
		31	$\overline{\text{TYDISL}}$	CU-2
		32	$\overline{\text{EXIOINH}}$	CU-2
		33	$\overline{\text{EXIOEND}}$	CU-2
		34	$\overline{\text{TYACCLD}}$	CU-2
CU-2	$\overline{\text{PAR}}$	35	$\overline{\text{TYCYCLE}}$	CU-2
		36		
		37	$\overline{\text{TYINST}}$	CU-2
		38	$\overline{\text{EXPAUSE}}$	CU-2
		39	$\overline{\text{TYCARRY IN}}$	CU-2
		40	$\overline{\text{EXIOCLK}}$	CU-2
		41		
		42		
		43	$\overline{\text{TYINC}}$	CU-2
MTC	MEMØ1	44	$\overline{\text{IOPCLD}}$	
MTC	MEMØ5	45	MEM1Ø	MTC
MTC	MEM11	46	MEMØ9	MTC

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

I/O SPARE

- P2 -

		A B		
CU-2	EXIOEN	47	MEMØ8	MTC
MTC	MEMØ3	48	MEMØ7	MTC
MTC	MEMØ2	49	MEMØ6	MTC
MTC	MEMØØ	50	MEMØ4	MTC

EXT ARITH

- P1 -

	+5V	1	GRD	
	+5V	2	GRD	
		3		
		4	EA PCEN	CU-2
CU-2	EAENMEM	5	EX-MEMEN	CU-1
CU-2	EARUN	6	EAIRCLR	CU-2
		7		
		8		
		9		
		10	EAENACCL	CU-2
CU-2	EAEND	11	EA-ENACC	CU-2
CU-2	EASTART	12		
CU-2, CU-1, SP	SLT4	13		
CU-1	IOACCØ2	14		
CU-1	IOACCØ1	15	IOACCØØ	CU-1
CU-2	OPR	16	EABUS11	CU-1
		17		
CU-2	PT3	18		
CU-2	PT2	19	BEXECUTE	CU-2
CU-2	PT2	20		
CU-1	EABUSØ1	21	PT3	CU-2
CU-1	EABUS1Ø	22	EABUSØ4	CU-1
		23		
		24		
CU-2	EAESET	25		
CU-2	BFETCH	26	PT4	CU-2
CU-1	EABUSØ5	27	EABUSØ9	CU-1
CU-1	EABUSØ2	28	EABUSØØ	CU-1
CU-1	EABUSØ8	29		
		30		
		31		
CU-1	EABUSØ6	32	EABUSØ7	CU-1
		33	EABUSØ3	CU-1
CU-2	BRUN	34	LT2	CU-2

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

EXT ARITH

- P1 -

		A B		
		35	$\overline{\text{POWER CLR}}$	CU-2
		36		
		37		
		38		
CU-1	BUMBRØ8	39		
CU-1	BUMBRØ6	40	BUMBRØ7	CU-1
CU-1	BUMBRØ4	41	BUMBRØ5	CU-1
		42		
		43	BLM2	CU-2

EXT ARITH

- P 2 -

		1	$\overline{\text{BLT3}}$	CU-2
CU-2	PM2	2	TLT1	CU-2
CU-1	$\overline{\text{IOACCØ9}}$	3		
CU-1	$\overline{\text{IO ACC1Ø}}$	4	$\overline{\text{IOACC11}}$	CU-1
		5		
		6		
CU-2	PM3	7	LT3	CU-2
CU-1	$\overline{\text{IOACCØ6}}$	8	$\overline{\text{LT4}}$	CU2, CU-1
CU-1	$\overline{\text{IOACCØ7}}$	9	$\overline{\text{IOACCØ8}}$	CU-1
CU-1	$\overline{\text{IOACCØ3}}$	10	$\overline{\text{IOACCØ4}}$	CU-1
		11	$\overline{\text{IOACCØ5}}$	CU-1
		12		
		13	PM1	CU-2
		14		
		15		
		16		
		17		
CU-1	BUMBRØ9	18		
CU-1	BUMBR1Ø	19	BUMBR11	CU-1
		20		
		21		
		22		
CU-2	BPAUSE	23		
		24		
		25		
		26		
		27		
		28		
		29		

TABLE 6-3. CONNECTOR PANEL PIN ASSIGNMENTS (Continued)

EXT ARITH

- P 2 -

		A	B		
		30			
		31			
		32		$\overline{\text{CLEAR}}$	CU-2
		33		$\overline{\text{EA EXECUTE}}$	CU-2
		34			
		35			
CU-2	$\overline{\text{EALDACC}}$	36		$\overline{\text{EADISL}}$	CU-2
CU-1	MEMØ9	37		MEM1Ø	CU-1
CU-1	MEMØ7	38		MEMØ8	CU-1
CU-1	MEMØ5	39		MEMØ6	CU-1
CU-1	MEMØ2	40		MEMØ4	CU-1
CU-1	MEM 11	41		MEMØ1	CU-1
CU-1	MEMØ3	42		MEMØØ	CU-1
	+5V	43		GRD	

SECTION VII

MEMORY EXTENSION AND CONTROL

1.0 GENERAL

The memory extension and control expands the memory capacity of the D-112 minicomputer from 4096-words up to a maximum of 32, 768 words. This option provides the three extra bits necessary for the addressing of 32K of memory.

2.0 DETAILED DESCRIPTION

The memory extension option provides two three bit registers, named Extended Instruction register and Extended Data register. The information stored in the three bit registers is controlled by the processor in order to supply the necessary addresses for additional memory. The Extended Instruction register is used whenever the processor references memory in fetching an instruction, or is used in referencing the address in memory where the address of the operand is stored during indirectly executed instructions. The extended data register is used only in indirect reference memory cycles (DEFER). Figure number 1 shows the three main states of the processor and indicates where each register is being used to reference memory.

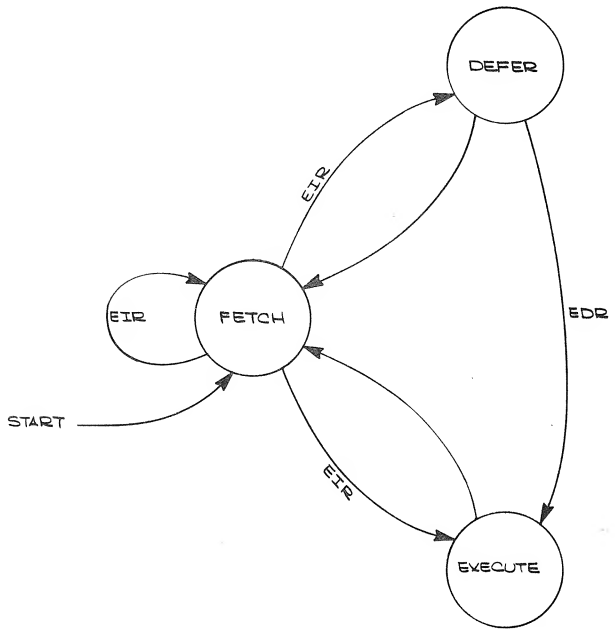


Figure 7-1

The outputs of these field registers are multiplexed and decoded by the memory extension and control, and finally encoded into eight field enable lines that control which core memory stack is being selected for the processor operation. For a more detailed description on all the registers and program operation of this option the D-112 User's Handbook should be consulted.

Following is a description of the logical operation of the memory extension control and its interface with the processor.

There are five main registers in its control logic. The extended instruction register (EIR) is a three bit register that contains the extended address for direct memory addressing. The extended data register (EDR) is a three bit register that contains the extended address for an indirect memory reference. The extended instruction buffer register is the three bit register that buffers all the information to be stored in the EIR register.

The Interrupt Save register (ISR) is seven bit register that saves the contents of the EIR, EDR, and user flag flip flop. Finally, the extended break field register (EBF) is a three bit register used to store the extended data address specified by a peripheral device during a data break operation.

The control section of the extended memory control has three main enable flip flops. They enable the input multiplexer, via its decode section to select one of the three main registers for address selection (EIR, EDR, or EBF). The extended memory control also provides an IOT decode section, which decodes all the necessary IOTs for software control of this option.

The control logic of this option can be divided into three main groups. The first group corresponds to the manual operation, which is under the control of the front panel switches of the processor. The second group will correspond to the control of the IOT instructions under control of the programmer, and is used for storing and reading information into the main registers of this option. Finally, there is internal control of this option where logic orders are determined according to the state of the processor and instruction being executed. The console operator can use the six switches provided in the front panel of the D-112 minicomputer to load information into the EIR, and EDR registers. This operation takes place when the load address key is pressed and provides a means to select the field addresses at which the program starts. When the load address key is pressed the signal K-LA is gated with the signal PM2 in order to produce the EIB-CLOCK and EDR-CLK loading signals. The signal BK-LA is generated by the load address key. It enables the LM-2 timing signal to produce the signal EX-SWR-EN which enables the contents of the data field switch register and instruction field switch register of the front panel into the EIB and EDR registers. These registers are loaded at PT2 time. The output of the EIB register is directly connected to the input of the EIR register and when the signal EIR-CLK signal is enabled at PM3 time by the load address key, the content of the instruction field switch is transfered into the extended instruction register (EIR).

3.0 MEMORY EXTENTION IOT's

The instructions utilized by this option employ the short cycle feature of the processor, hence they do not generate the IOP timing pulses. The execution time of these instructions corresponds to one memory cycle (1.2 microseconds).

3.1 CHANGE TO DATA FIELD (CDF)

This instruction 62N1 (Octal) loads the extended data register with the contents of the MBR bits 06, 07 & 08. After this instruction all indirect memory requests for an operand are automatically switched to that data field until the contents of this register are changed by another CDF command, or by the execution of a program interrupt.

The signal MEMEXTIOT is enabled whenever an IOT refers to the memory extension control option. This signal gated with MBR 11 generates the signal BF62X1 which at LT3 time enables the memory buffer register bits 6, 7, 8 into the input of the EDR register. At PT3 time, the signal BF62X1 also enables the loading signal EDRCLK that loads the contents of the memory buffer register into the extended data register, completing the transfer of information at this time.

3.2 CHANGE TO INSTRUCTION FIELD (CIF)

This instruction 62N2 (Octal) loads the contents of MBR06, 07, 08 into the extended instruction buffer register. The signal BF62X2 is decoded during this instruction and is gated with LT3 in order to produce the signal EIN-MBR-EN. This signal enables the memory buffer register bits 6, 7, 8 into the data input of the EIB register. BF72X2 is also gated with PT3 in order to produce the EIB-CLK clock that stores the contents of the MBR into the EIB register.

The same signal that enables the MBR into the buffer register will set the INT control flip flop. This flip flop will set the signal INTCONT. This inhibits interrupts to processor until the execution of a JMS or JMP instruction.

The contents of the extended buffer register is transferred into the extended instruction register during the execution of the JMS or JMP instruction. The decodes of these instructions are gated with PT3 in order to set the EIR-CLK delay FF. This flip flop enables the signal EIR-CLK at PT4 time, which loads the contents of the extended instruction buffer register into the extended instruction register. This flip flop provides a delay of one computer sub-cycle before this transfer in order to save the address of the field contained by the extended instruction register of the current cycle. The EIR-CK-DELAY flip flop is cleared by the lagging edge of PT4. The same timing pulse that set the delay flip flop will clear the INT CONTROL flip flop that enables the interrupt request line into the processor.

3.3 READ DATE FIELD (RDF)

This instruction 6214 (Octal) transfers the contents of the extended data field register ORed into bits 6, 7, 8 of the ACC.

The signal 6214 is decoded and enables the contents of the external data field register (EDR) onto the internal I/O bus of the processor. The information stored in this register will be applied to the internal I/O thru the INT I/O-6, INT I/O-7, and INT I/O-8 of the I/O board. The 6214 signal also enables two control signals EXIONEN at LT3 and MEACCLD at PT3. EXIONEN enables the internal I/O of the processor into input multiplexer B of the computer, and MEACCLD loads this information into the Accumulator. During the I/O operation of the processor the accumulator is also enabled into the input multiplexer B providing the OR of both registers.

3.4 READ INSTRUCTION FIELD (RIF)

This instruction 6224 (Octal) transfers the contents of the extended instruction field register (ORed) with the contents of the accumulator into bits 6, 7, 8. The other bits of the accumulator are not affected. The IOT decode 6224 enables the contents of the EIR register onto the internal bus of the processor. The 6224 signal also enables the EXIONEN, and MEACLLD signals which perform the same operation as the instruction described previously.

3.5 READ INTERRUPT BUFFER (RIB)

This instruction 6234 (Octal) performs a similar operation to the two previous instructions. The signal 6234 is enabled by the decode section of the Memory Extension (ME), and enables the seven bits of the ISR register onto the internal I/O bus of the processor. INT I/O 6 thru INT I/O-11 are Ored with the same bits of the accumulator during the execution of this instruction. The signals EXIOEN and MEACCLD are enabled during this instruction in order to perform the same operation as previously described. The other bits of the accumulator remain unchanged during this operation.

3.6 RESTORE MEMORY FIELD (RMF)

This instruction 6244 (Octal) is used for sub-routines when an exit from the program interrupt is being effected. The data and instruction field registers that were saved by the ISR register during the interrupt request to the processor are restored to their respective registers by this instruction. This is done in order to restore the previous status of the machine before the interrupt request was answered. The signal 6244 decoded by the IOT section enables, at Lt3 time, the multiplexer enable signal EX-ADD-SREN. This gates the interrupt save register into the extended data register (EDR) and the extended buffer register (EIB). At PT3 time the signals EIBCLK and EDRCLK are also produced by the 6244 decode. These two signals transfer the information of the ISR register into the EIR and EDR registers. The contents of the extended instruction register EIR is not immediately altered by this operation. This register will be up-dated with the information stored in the EIR register when a jump or JMS instruction is executed by the program.

4.0 MEMORY EXTENSION INTERNAL CONTROL

The internal control of the memory extension is provided by three main control flip flops. They are the EBF and EIR enable flip flops. These flip flops will decode which register is to be used to specify the address field of the core stack. When a deposit key, examine key or start key is depressed these signals are Anded with PM2 in order to provide a unique clock for these three flip flops. The D inputs of the flip flops are controlled by a series of logic signals from the processor, and determine which of them will be set for the next operation of the computer. The signal EIRSET when asserted sets the EIR flip flop in order to enable the EIR register. This signal is always enabled whenever the two D inputs of the EBF and EDF flip flops are disabled. This signal is inhibited when the processor is in word count state or the processor is in the state (DWCSET and BDWC). When the START key is pressed the EIR flip flop is set supplying to the field decode section of the extended memory the contents of the EIR register. This register specifies the address of the field stack to be used in the fetch cycle of the processor. At PT4 time the clock signals of the three flip flops (MECLK) will be also issued by the control. The transition of control from one flip flop to another can take place according to the state of the control logic in the processor at this time. If the processor is answering the three cycle data break, the signals DWCSET, or BDWC will inhibit the EIR flop at PT4 time. This operation clears the three control flip flops. The field address register decoder is disabled, hence field zero is enabled under these conditions. This operation results in the enabling of memory field zero for the word count, and current address cycles of the data break. The contents of the EDF and EIR, register remain unchanged. In order to set the processor into the break state, the signal DCC set must be enabled and the EDF enable flip flop set. The address specified by the peripheral device requesting the data break is then decoded. The information in the EBF register is then stored at PT3 time. The data input of this register is supplied by three extended address lines supplied by the peripheral devices. The EDFSET signal that enables the EBF enable flops inhibits the EIR flop from being set. The EDF enable flop is only enabled at the end of the Defer cycle at PT4 time (indirect address), if JMP or JMS instructions are not being executed by the processor.

When the processor is answering an interrupt request from a device, the signal ISRCLK, is generated by the LT1 and INT signals. The function of this signal is to load the contents of the EDR and EIR register into the interrupt save register (ISR). The SIRCLK signal also generates three clear signals, EIBCLR, EDRCLR and EIRCLR. This clears the respective registers after the information is transfered into the ISR register. These three clear signals are inhibited by the signal EXMEMCLR if an IOT is being processed to turn off the interrupt system of the computer.

The control section of the Memory Extension Control also provides updating of the extended instruction register, under program control, in order to allow the programmer to jump from one memory stack to another. This occurs at PT3 time and is enabled by the JMP or JMS signals during FSET and ESET.